Access DB# 123815

SEARCH REQUEST FORM

Scientific and Technical Information Center

24

Requester's Full Name: _Jack Lane_____ Examiner # :68699___ Date: _6/2/04_____
Art Unit: 2188_ Phone Number 305-3818___ Serial Number: 09/843,228___
Mail Box Location: _2Y13___ Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: ___Low Latency inter-reference ordering in a multiple processor system employing a multiple-level inter-node switch.____

Inventors (please provide full names): _Simon C. Steely JR., Madhumitra Sharma and Stephen R. Van Doren

Earliest Priority Filing Date: 04/26/01_____

For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.

See Abstract and claims.

Search:

Switch and node
Message
Atomic message

****

STAFF USE ONLY

Searcher: Terese Estenfeld
Searcher Phone #: 308-7796
Searcher Location: 4B 30
Date Searcher Picked Up: 6/9/04 9:45am
Date Completed: 6/10/04 8:50am
Searcher Prep & Review Time: _____

Type of Search

NA Sequence (#)_____
AA Sequence (#)_____
Structure (#) _____
Bibliographic _____
Litigation _____
Fulltext _____

Vendors and cost where applicable

STN _____
Dialog _____
Questel/Orbit _____
Dr.Link _____
Lexis/Nexis_____
Sequence Systems _____

STIC Search Report
EIC 2100

STIC Database Tracking Number: 123815

TO:	From:
John Lane **Location: 2Y13** **Art Unit : 2188** **Thursday, June 10, 2004** **Case Serial Number: 09/843228**	**Terese Esterheld** **Location: EIC 2100** **PK2-4B30** **Phone: 308-7795** **Terese.esterheld@uspto.gov**

Search Notes

Dear Examiner Lane,

Attached, please find the results of your search request for application 09/843228. I have concentrated on finding information on Inter node switches, Switches, Nodes and Atomic messages.

Please over the complete package, particularly the full text Non Patent Literature, as there appear to be citations of value to you.

Please let me if you need additional information on this search.

Thank you for coming to EIC 2100.

Terese Esterheld

STIC Search Results Feedback Form

EIC 2100

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact***:

Anne Hendrickson, EIC 2100 Team Leader
308-7831, CPK2-4B40

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2133*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2100 CPK2-4B40

```
Set     Items   Description
S1          6   (INTERNODE? OR INTER()NODE?)(2W)SWITCH?
S2    1547308   SWITCH? OR INTERFACE? OR PROTOCOL? OR ADAPTER? OR CONTROL(-
              )DEVICE? OR ROUTER? OR BRIDGE? OR MULTIPLAYER?
S3    5411524   NODE? OR CLIENT? OR STAND()ALONE? OR STANDALONE? OR PC OR -
             WORKSTATION? OR WORK()STATION? OR COMPUTER? OR NETWORK? OR LAN
              OR LANS OR INTRANET? OR PROCESSOR? OR HOST? OR SERVER? OR CPU
              OR MICROCOMPUTER?
S4    7103156   MESSAGE? OR DATA OR INFORMATION OR TRANSACTION? OR PACKET?
             OR (E OR ELECTRONIC)()MAIL OR EMAIL OR TEXT
S5        653   ATOMIC (2N) S4
S6     368168   S2 (S) S3 (S) S4
S7          3   S6 (S) S1
S8         30   S2 (S) S3 (S) S5
S9          0   S8 (S) S1
S10         0   S5 (S) S1
S11        36   S1 OR S7 OR S8
S12        32   S11 NOT PY>2001
S13        30   S12 NOT PD>20010426
S14        28   RD (unique items)
File 647:CMP  Computer Fulltext 1988-2004/May W5
         (c) 2004 CMP Media, LLC
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 09
         (c) 2004 The Gale Group
File 674:Computer News Fulltext 1989-2004/May W5
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 08
         (c) 2004 The Dialog Corp.
File 624:McGraw-Hill Publications 1985-2004/Jun 09
         (c) 2004 McGraw-Hill Co. Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jun 07
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jun 08
         (c) 2004 The Gale Group
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 613:PR Newswire 1999-2004/Jun 09
         (c) 2004 PR Newswire Association Inc
```

14/3,K/1 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

01126708 CMP ACCESSION NUMBER: NWC19970515S0028
Web Middleware Glue Binds Web Apps
Barry Nance
NETWORK COMPUTING, 1997, n 809, PG107
PUBLICATION DATE: 970515
JOURNAL CODE: NWC LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Corporate.Net
WORD COUNT: 3915

... middleware works with Java-capable Web browser clients and supports both Java and ActiveX.
We found Enterprise **Server** , like the other products in this review, consists of a transaction and request manager, several APIs for...

...The transaction and request manager relies on state and session information to manage multistep, complex requests as **atomic transactions** . The administrative tools gave us a graphical **interface** for managing distributed application components and transactions in a run-time environment. We noted the security module...

14/3,K/4 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

02105619 SUPPLIER NUMBER: 19805220
Can LDAP handle atomic transactions? (Lightweight Directory Access Protocol) (Technology Information)(Interview)
Hudgins-Bonafield, Christy
Network Computing, v8, n18, p30(2)
Oct 1, 1997
DOCUMENT TYPE: Interview ISSN: 1046-4468 LANGUAGE: English
RECORD TYPE: Abstract

...ABSTRACT: transactions over Lightweight Directory Access Protocol (LDAP) have formed a group to determine whether LDAP can support **atomic** operation of **transaction** processing. The question of **atomic transactions** , which refer to uninterruptible or completely aborted operations, was first discussed at the Aug 1997 meeting of...

...handle any transactions. Such an LDAP extension would then raise the question of either transmitting across single **server** transactions or replicas, plus the transaction's quality. Another issue consists of defining a transaction as a...

14/3,K/7 (Item 6 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01692943 SUPPLIER NUMBER: 16057410 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Corporate business servers: an alternative to mainframes for business computing. (HP's 9000 Model T500 file server) (includes related article on package designing) (Technical)
Alexander, Thomas B.; Robertson, Kenneth G.; Lindsay, Dean T.; Rogers, Donald L.; Obermeyer, John R.; Keller, John R.; Oka, Keith Y.; Jones, Marlin M., II
Hewlett-Packard Journal, v45, n3, p8(23)
June, 1994
DOCUMENT TYPE: Technical ISSN: 0018-1153 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 16095 LINE COUNT: 01283

... the system to achieve excellent online transaction processing (OLTP) performance and efficient multiprocessor scaling.

Bus Protocol

The **processor** memory bus is a synchronous pipelined bus. The pipelined nature of the bus **protocol** places it between a split transaction **protocol** and an **atomic transaction protocol** . This allows the **processor** memory bus to have the performance of a split transaction bus with the lower implementation complexity of an **atomic transaction** bus.

The processor memory bus has separate address and data buses. The address bus is used to...

14/3,K/9 (Item 8 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01632508 SUPPLIER NUMBER: 14812079 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Global positioning system packs platform-independent PCMCIA interface. (Mobile GPS Sensor codeveloped by Trimble Navigation and Socket Communications) (Special OEM Integration supplement)
Computer Design, v32, n11, pOEM-2(2)
Nov, 1993
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 482 LINE COUNT: 00040

...ABSTRACT: air and sea navigation systems, natural resource management, inventory control, emergency disaster response systems, consumer guides, and **network** synchronization. The GPS will satisfy the requirements for any application that requires accurate Absolute **Atomic** Time **Data** and geographic position data. The device, jointly developed by Socket Communications and Trimble Navigation, includes a six...

14/3,K/13 (Item 12 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01314845 SUPPLIER NUMBER: 07834400 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Open Server: Sybase opens up.
RELease 1.0, v89, n10, p11(2)
Oct 17, 1989
ISSN: 1047-935X LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1199 LINE COUNT: 00094

... of SQL Server.

The Open interface

Sybase is trying to establish a standard way of communicating between **clients** and **servers** . The primary models are Sybase's own front-end tools and SQL **Server** . Open **Server** and Open **Client** contain toolkits and intermediary **interfaces** which handles communications, etc., so that users needn't be concerned with system underpinnings (once someone has built and installed the **server** and **client** components using the toolkits). It also provides **protocols** for calling "database RPCs," which can manipulate whole tables and other data types as well as the **atomic data** typically handled by RPCs, and which can call other database RPCs.

While SQL Server handles relational data...

14/3,K/14 (Item 13 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01221528 SUPPLIER NUMBER: 06573213
Recovery management in QuickSilver.
Haskin, Roger; Malachi, Yoni; Sawdon, Wayne; Chan, Gregory
ACM Transactions on Computer Systems, v6, n1, p82(27)
Feb, 1988

ISSN: 0734-2071 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

...ABSTRACT: called QuickSilver, which was developed at the IBM Almaden Research Center in San Jose, California. QuickSilver employs **atomic transactions** as a unified failure recovery mechanism for a **client - server** structure distributed system. The system exposes the basic commit **protocol** and log recovery primitives to allow both **clients** and **servers** to tailor recovery techniques to suit their individual need.

14/3,K/15 (Item 14 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01172668 SUPPLIER NUMBER: 00666125
A blueprint for business architectures.
Strobl, Rudolf; Stackhouse, Bill
Data Communications, v15, n3, p151-154
March, 1986
ISSN: 0363-6399 LANGUAGE: ENGLISH RECORD TYPE: ABSTRACT

ABSTRACT: Information **network** architectures (INAs) are intended to overcome the isolation of different **network protocols** to allow each environment to communicate with the other by separating business application programs from the communications support structure and providing them with a common **interface** for end-to-end services. To do this, the application layer is divided into three layers: business functions, delivery and control functions, and **network** service functions. Components of the business function layer include **atomic transactions** , error management, file transfer services, software distribution, universal electronic mailboxes, and library services. The delivery and control layer includes levels of service, global **network** directories, translation and transformations, notification procedures, security, and recovery management. The **network** services layer insulates investments in code written for business functions and delivery and control functions from the **computer** hardware environment and public and proprietary data communications **protocols** . CAPTION: (Eight diagrams show the components of the INA system.)

14/3,K/18 (Item 3 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2004 The Gale Group. All rts. reserv.

01790347 Supplier Number: 53585521 (USE FORMAT 7 FOR FULLTEXT)
Atomic Software and GTE Wireless Announce Branding Agreement.
Business Wire, p0147
Jan 18, 1999
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 365

... 12-30 seconds using a traditional phone line. CDPD service is available in most major metropolitan areas.
" **PC** -Retailer will provide electronic payment capability to mobile merchants that were heretofore unable to collect guaranteed payments...

...of Atomic Software. "Moreover, it opens new markets such as fast food stores with its lightning fast **transaction** times."
Atomic Software will also provide and support an Application Program Interface to software developers who wish to integrate...

14/3,K/19 (Item 4 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2004 The Gale Group. All rts. reserv.

01617002 Supplier Number: 48335152 (USE FORMAT 7 FOR FULLTEXT)

SPC Joins MicroStrategy's DSS Partners Program.
Business Wire, p3041163
March 4, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 690

... suite to be the most comprehensive and scalable offering on the market, with DSS Agent, the MicroStrategy **interface** , providing the detailed querying capabilities necessary for SPC's rigorous **client** demands. Using MicroStrategy technology, **clients** can explore trends and **transactions** at the **atomic** **data** level and use that information to better understand their businesses.
"MicroStrategy's tools provide SPC with the...

14/3,K/20 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03834789 Supplier Number: 48328626 (USE FORMAT 7 FOR FULLTEXT)
MICROSTRATEGY: ProLink Services L.L.C. teams with MicroStrategy in systems integrator agreement
M2 Presswire, pN/A
March 2, 1998
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 855

... end users to compile ad hoc reports from remote locations, while DSS Executive offers a simplified GUI **interface** tailored to an end user's specific reporting needs. With these sophisticated DSS tools, ProLink can now offer its **clients** technology that will enable them to achieve optimum business performance through enhanced profitability, streamlined operations, and more...

14/3,K/21 (Item 2 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

03799506 Supplier Number: 48237411 (USE FORMAT 7 FOR FULLTEXT)
Highly-Parallel Operating Systems
High Performance Computing & Communications Week, v7, n3, pN/A
Jan 20, 1998
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 1211

... multiple words (i.e., on multiword RMW).
People studying this problem have proposed stealing the notions of **atomic** **transactions** and optimistic concurrency control from the database community. Given their faith in stock **processors** with a single program counter, they invariably come up with some variation of the **processor** 's hardware-managed invalidation-based cache-coherence **protocol** . Let's try a somewhat different implementation of lock-free **atomic** **transactions** with no critical sections!
Say a transaction in a parallel program depends on two independent data sets...

```
Set      Items   Description
S1          26   (INTERNODE? OR INTER()NODE?)(2W)SWITCH?
S2     1783697   SWITCH? OR INTERFACE? OR PROTOCOL? OR ADAPTER? OR CONTROL(-
             )DEVICE? OR ROUTER? OR BRIDGE? OR MULTIPLAYER?
S3     4756241   NODE? OR CLIENT? OR STAND()ALONE? OR STANDALONE? OR PC OR -
            WORKSTATION? OR WORK()STATION? OR COMPUTER? OR NETWORK? OR LAN
             OR LANS OR INTRANET? OR PROCESSOR? OR HOST? OR SERVER? OR CPU
             OR MICROCOMPUTER?
S4     5690287   MESSAGE? OR DATA OR INFORMATION OR TRANSACTION? OR PACKET?
            OR (E OR ELECTRONIC)()MAIL OR EMAIL OR TEXT
S5        5669   ATOMIC (2N) S4
S6      351303   S2 AND S3 AND S4
S7          16   S6 AND S1
S8         202   S2 AND S3 AND S5
S9          91   (S2 (5N) S3)AND S5
S10        107   S7 OR S9
S11         98   S10 NOT PY>2001
S12         98   S11 NOT PD>20010426
S13         81   RD (unique items)
File   8:Ei Compendex(R) 1970-2004/May W5
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Jun W1
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/May W5
         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File  94:JICST-EPlus 1985-2004/May W3
         (c)2004 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/May W4
         (c) 2004 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
```

13/5/5 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05560420 E.I. No: EIP00055170744
Title: Web-based workflow management system
Author: Ye, Xinfeng
Corporate Source: Auckland Univ, Auckland, New Zealand
Conference Title: 1999 IEEE International Conference on Systems, Man, and Cybernetics 'Human Communication and Cybernetics'
Conference Location: Tokyo, Jpn Conference Date: 19991012-19991015
Sponsor: IEEE (SMC); SCJ; SICE; RSJ; JSME
E.I. Conference No.: 56750
Source: Proceedings of the IEEE International Conference on Systems, Man and Cybernetics v 1 1999. IEEE, USA. p I-910 - I-915
Publication Year: 1999
CODEN: PICYE3 ISSN: 0884-3627
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications)
Journal Announcement: 0007W1
Abstract: This paper describes a web-based workflow management system for a rental car company. Web browsers are the interface between the system and the users. The system consists of two types of tasks: transactional and non-transactional. The **transactional** tasks are **atomic transactions** . They can access more than one database. Thus, the system provides atomic operations on multiple databases. (Author abstract) 8 Refs.
Descriptors: Office automation; World Wide Web; Web browsers; User **interfaces** ; Database systems; **Computer** supported cooperative work; **Network protocols** ; Java programming language; Electronic mail; HTML
Identifiers: Workflow management system; Rental car company
Classification Codes:
723.1.1 (Computer Programming Languages)
723.5 (Computer Applications); 912.2 (Management); 722.2 (Computer Peripheral Equipment); 723.3 (Database Systems); 723.1 (Computer Programming)
723 (Computer Software); 912 (Industrial Engineering & Management); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

13/5/13 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04958681 E.I. No: EIP98034096899
Title: Supercomputer SX-4 multinode system
Author: Hori, Kenichi
Corporate Source: 1st Computers Software Div
Source: NEC Research & Development v 38 n 4 Oct 1997. p 461-473
Publication Year: 1997
CODEN: NECRAU ISSN: 0547-051X
Language: English
Document Type: RR; (Report Review) Treatment: G; (General Review)
Journal Announcement: 9804W5
Abstract: The NEC supercomputer SX-4 multinode system series consists of two models, one being HIPPI (High Performance Parallel **Interface**)-connected model and the other IXS (**Internode** Crossbar **Switch**)-connected model. With the IXS, a proprietary high-speed crossbar **switch** , the HPC (High Performance Computing) up to 1 TFLOPS (Tera Flops) has been enabled by providing the most comprehensive environment for distributed parallel processing. This also means the world's first implementation of a clustered parallel processing. In this paper, we describe the functions of IXS hardware, the new operating system functions, MPI/SX the MPI (**Message** Passing **Interface**) **processor** and NQS/MPI which supports the close cooperation between NQS (**Network** Queuing System) batch processing system and MPI. (Author abstract) 3 Refs.
Descriptors: Supercomputers; Parallel processing systems; **Interfaces** (

computer); **Computer** operating systems; **Computer** hardware; **Computer networks** ; FORTRAN (programming language)
Identifiers: High performance computing (HPC); **Message** passing **interface** (MPI); High performance parallel **interface** (HPPI); Clustered parallel processing; Shared memory **computer** systems
Classification Codes:
723.1.1 (Computer Programming Languages)
722.4 (Digital Computers & Systems); 722.2 (Computer Peripheral Equipment); 722.1 (Data Storage, Equipment & Techniques); 722.3 (Data Communication, Equipment & Techniques); 723.1 (Computer Programming)
722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

13/5/25 (Item 25 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04258714 E.I. No: EIP95102879082
Title: Context-specific synchronization for atomic data **types in object-based databases**
Author: Wong, Man Hon; Agrawal, Divyakant
Corporate Source: Chinese Univ of Hong Kong, Hong Kong
Source: Theoretical Computer Science v 149 n 1 Sept 18 1995. p 179-199
Publication Year: 1995
CODEN: TCSCDI ISSN: 0304-3975
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9511W4
Abstract: Highly concurrent and reliable **atomic data** types are crucial for object-based databases. Deferred update (DU) and update-in-place (UIP) are two common recovery-strategies for implementing **atomic data** types. These two strategies place incomparable constraints on the conflict relations between concurrent operations resulting in incomparable synchronization protocols. Also, the conflict relations used are usually static in the sense that they depend only on the operation types, and the algorithms do not use the context-specific information that may be available in the system. In this paper, a new synchronization mechanism that employs a hybrid scheme by using both DU and UIP is proposed. Furthermore, the protocol is dynamic in the sense that context-specific information is also used to determine conflict relations among concurrent operations. Another extension is the use of ordered shared relationships between locks to execute conflicting operations concurrently. The execution of operations is never delayed in the proposed protocol, however, the commitment of the transactions invoking these operations may be delayed due to the restriction imposed by the ordered shared relationships between locks. It is demonstrated that the sets of histories accepted by the two phase locking protocols using DU or UIP are proper subsets of the set of histories accepted by the proposed protocol. (Author abstract) 17 Refs.
Descriptors: Database systems; Synchronization; Data structures; Concurrency control; Constraint theory; **Network protocols** ; Algorithms
Identifiers: Context specific synchronization; Context specific **information** ; **Atomic data** types; Object based databases; Deferred update; Update inplace; Ordered shared relationships; Phase locking protocols
Classification Codes:
723.3 (Database Systems); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory); 723.2 (Data Processing); 921.6 (Numerical Methods)
723 (Computer Software); 721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

13/5/26 (Item 26 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

04201226 E.I. No: EIP95062761384
Title: Allnode barrier synchronization network
Author: Olnowich, Howard T.
Corporate Source: IBM Corp, Endicott, NY, USA
Conference Title: Proceedings of the IEEE 9th International Parallel Processing Symposium
Conference Location: Santa Barbara, CA, USA Conference Date: 19950425-19950428
Sponsor: IEEE
E.I. Conference No.: 43165
Source: IEEE Symposium on Parallel and Distributed Processing - Proceedings 1995. IEEE, Los Alamitos, CA, USA,95TH8052. p 265-269
Publication Year: 1995
CODEN: PSPDF8 ISSN: 1063-6374
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications)
Journal Announcement: 9509W1
Abstract: This paper presents a proposed hardware solution using an existing multi-stage **switching network** for synchronizing N multiple **processors** at predetermined programmable barriers. The technique permits all N **processors** to access the **network** simultaneously and to perform synchronization in parallel using only several **network** cycles. The synchronization requires no additional **network** facilities, and consumes usually less than 5% of the bandwidth when merged onto the same multi-stage **network** that handles normal **message** traffic. The approach permits up to 2048 barriers, but can be expanded. The **network** is based on the Allnode **Switch** and **Network** concepts left bracket 1 right bracket , a circuit-**switching** implementation, that permits a special barrier synchronization mode where all N **processors** are simultaneously attached to the **network** and can interact as if they were attached to a multi-drop bus. (Author abstract) 8 Refs.
Descriptors: **Switching networks** ; **Computer** hardware; Parallel processing systems; Synchronization; **Data** communication systems; Buffer storage
Identifiers: Barrier synchronization **network** ; Asynchronous low latency **inter node switch** ; **Message** passing **network**
Classification Codes:
722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques)
721 (Computer Circuits & Logic Elements); 722 (Computer Hardware); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

13/5/29 (Item 29 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04136624 E.I. No: EIP95031602956
Title: Single logical view over enterprise-wide distributed databases
Author: Wade, Andrew E.
Corporate Source: Objectivity, Inc
Conference Title: Proceedings of the 1993 ACM SIGMOD International Conference on Management of Data
Conference Location: Washington, DC, USA Conference Date: 19930526-19930528
Sponsor: ACM, SIGMOD; Minerals & Metals & Materials Society
E.I. Conference No.: 19810
Source: SIGMOD Record (ACM Special Interest Group on Management of Data) v 22 n 2 Jun 1993. Publ by ACM, Fort Collins Computer Center, Fort Collins, CO, USA. p 441-444
Publication Year: 1993
CODEN: SRECD8 ISSN: 0163-5808 ISBN: 0-89791-592-5
Language: English

Document Type: CA; (Conference Article) Treatment: G; (General Review)
Journal Announcement: 9506W2
Abstract: Two trends in today's corporate world demand distribution: downsizing from centralized mainframe single database environments; and wider integration, connecting finance, engineering, manufacturing information systems for enterprise-wide modeling and operations optimization. The resulting environment consists of multiple databases, at the group level, department level, and corporate level, with the need to manage dependencies among data in all of them. The solution is full distribution, providing a single logical view to objects anywhere, from anywhere. Users see a logical model of objects connected to objects, with **atomic transactions** and propagating methods, even if composite objects are split among multiple databases, each under separate administrative control, on multiple, heterogeneous platforms, operating systems, and **network protocols** . Support for production environments includes multiple schemas, which may be shared among databases, private, or encrypted, dynamic addition of schemas, and schema evolution. Finally, the logical view must remain valid, and applications must continue to work, as the mapping to the physical environment changes, moving objects and databases to new platforms. (Author abstract)
Descriptors: Distributed database systems; Object oriented programming; Management information systems; **Computer** simulation; **Computer** operating systems; **Network protocols** ; C (programming language); Data structures; Optimization
Identifiers: Single logical view; Enterprise wide distributed databases; Schema; Object database management system; Objectivity
Classification Codes:
723.3 (Database Systems); 723.1 (Computer Programming); 912.2 (Management); 723.5 (Computer Applications); 722.4 (Digital Computers & Systems); 722.3 (Data Communication, Equipment & Techniques)
723 (Computer Software); 912 (Industrial Engineering & Management); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

13/5/41 (Item 41 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03554981 E.I. Monthly No: EI9302017610
Title: Fault impact and fault tolerance in multiprocessor interconnection networks .
Author: Menezes, Bernard; Johnson, Allen M. Jr.; Malek, Miroslaw; Jenevein, Roy; Yau, Kitty H.
Corporate Source: Univ of Maryland, College Park, MD, USA
Source: Quality and Reliability Engineering International v 8 n 5 Sep-Oct 1992 p 485-500
Publication Year: 1992
CODEN: QREIE5 ISSN: 0748-8017
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9302
Abstract: Growing complexity of parallel machines coupled with increasing chip densities escalates the need for fault tolerance and recovery in these systems. In pursuit of the goal of fault-tolerant multiprocessors, many techniques have been proposed. Since methods for designing fault-tolerant **processors** and memories are relatively mature, the techniques considered in this paper focus on the interconnection **network** (ICN) linking the **processors** . The impact of faults on non-fault-tolerant ICNs is contrasted with that in fault-tolerant **networks** . Fault tolerance in ICNs is addressed at two levels, **inter - node** or **switch** level and system level. **Inter - node** or **switch** level pertains to **data** and control integrity and system level deals with maintaining **network** connectivity and adequate performance levels in the presence of faults. Fault-tolerant schemes at the **switching** element level warrant some form of concurrent error detection such as the use of codes usually combined with a full handshake **protocol** .

Space-time trade-offs involved in the use of various codes and **protocols** are investigated. At the system level, several augmented multi-stage **switching** ICNs, tree and ring **networks** are studied. The combined provision for fault tolerance together with improved performance in the non-fault condition is emphasized. Finally, strategies for **network** reconfiguration and rerouting after system failure are presented. (Author abstract) 45 Refs.

Descriptors: FAULT TOLERANT **COMPUTER** SYSTEMS; PARALLEL PROCESSING SYSTEMS; FAILURE ANALYSIS; **SWITCHING NETWORKS** ; **NETWORK PROTOCOLS** ; ERROR DETECTION; PERFORMANCE

Identifiers: CONCURRENT ERROR DETECTION (CED); **DATA** INTEGRITY; FAULT MODEL; **NETWORK** BANDWIDTH; SPATIAL REDUNDANCY; TEMPORAL REDUNDANCY

Classification Codes:

722 (Computer Hardware); 703 (Electric Circuits); 723 (Computer Software); 921 (Applied Mathematics)

72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING); 92 (ENGINEERING MATHEMATICS)

13/5/43 (Item 43 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

03001779 E.I. Monthly No: EIM9012-051688

Title: Reliable distributed computing with Avalon/Common Lisp.

Author: Clamen, Stewart M.; Leibengood, Linda D.; Nettles, Scott M.; Wing, Jeannette M.

Corporate Source: Sch of Comput Sci, Carnegie Mellon Univ, Pittsburgh, PA, USA

Conference Title: 1990 International Conference on Computer Languages

Conference Location: New Orleans, LA, USA Conference Date: 19900312

Sponsor: IEEE Computer Soc, Computer Languages Technical Committee, New Orleans, LA, USA

E.I. Conference No.: 13804

Source: 1990 Int Conf Comput Lang. Publ by IEEE, Computer Society, Los Alamitos, CA, USA (IEEE cat n 90CH2854-8). p 169-179

Publication Year: 1990

ISBN: 0-8186-2036-6

Language: English

Document Type: PA; (Conference Paper) Treatment: X; (Experimental)

Journal Announcement: 9012

Abstract: An overview of these novel aspects of Avalon/Common Lisp is presented: (1) support for remote evaluation through a new evaluator data type; (2) a generalization of the traditional client/server model of computation, allowing **clients** to extend **server interfaces** and **server** writers to hide aspects of distribution, such as caching, from clients; (3) support for failure atomicity through automatic commit and abort processing of transactions; and (4) support for persistence through automatic crash recovery of **atomic data** . These capabilities provide programmers with the flexibility to exploit the semantics of an application to enhance its reliability and efficiency. Avalon/Common Lisp runs on IBM RTs on the Mach operating system. Though the design of Avalon/Common Lisp exploits some of the features of Common Lisp, e.g., its packaging mechanism, all of the constructs are applicable to any Lisp-like language. 26 Refs.

Descriptors: *COMPUTER PROGRAMMING LANGUAGES--*LISP; COMPUTER SYSTEMS, DIGITAL--Distributed; COMPUTER SYSTEMS PROGRAMMING--Multiprocessing Programs

Identifiers: AVALON/COMMON LISP; REMOTE EVALUATION; FAILURE ATOMICITY; AUTOMATIC CRASH RECOVERY

Classification Codes:

723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING)

13/5/44 (Item 44 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

02958585 E.I. Monthly No: EIM9009-038061
Title: Monitoring database objects.
Author: Risch, Tore
Corporate Source: Hewlett-Packard Lab, Palo Alto, CA, USA
Conference Title: Proceedings of the Fifteenth International Conference on Very Large Data Bases
Conference Location: Amsterdam, Neth Conference Date: 19890822
E.I. Conference No.: 13326
Source: Very Large Data Bases, International Conference on Very Large Data Bases. Publ by Morgan Kaufmann Publ Inc, Los Altos, CA, USA. p 445-453
Publication Year: 1989
CODEN: VLDBDP
Language: English
Document Type: PA; (Conference Paper) Treatment: A; (Applications)
Journal Announcement: 9009
Abstract: A method is described for actively interfacing an Object-Oriented Database Management System (OODBMS) to application programs. The method, called a database monitor, observes how values of derived or stored attributes of database objects change over time. Whenever such a value change is observed, the OODBMS invokes tracking procedures within running application programs. The OODBMS associates tracking procedures and the object attributes they monitor, and it invokes appropriate tracking procedures when data changes. Use is made of **atomic transactions** in the OODBMS. (Edited author abstract) 32 Refs.
Descriptors: DATABASE SYSTEMS--* **Computer Interfaces** ; **COMPUTER** SOFTWARE--Applications
Identifiers: OBJECT-ORIENTED DATABASES
Classification Codes:
723 (Computer Software); 722 (Computer Hardware)
72 (COMPUTERS & DATA PROCESSING)

13/5/62 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5056472 INSPEC Abstract Number: B9511-6150M-002, C9511-5640-003
Title: The ODBMS role in 64 bit distributed client-server computing
Author(s): Wade, A.E.
Author Affiliation: Objectivity Inc., Menlo Park, CA, USA
Conference Title: Conference Proceedings Combined Volumes. Electro/94 International (Cat. No.94CH35789) p.603-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1994 Country of Publication: USA 963 pp.
ISBN: 0 7803 2630 X
Conference Title: Proceedings of ELECTRO '94
Conference Sponsor: IEEE
Conference Date: 10-12 May 1994 Conference Location: Boston, MA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Two trends in today's corporate world demand distribution: downsizing from centralized mainframe single-database environments; and wider integration, connecting finance, engineering, and manufacturing information systems for enterprise-wide modeling and operations optimization. The resulting environment consists of multiple databases, at the group level, department level, and corporate level, but with the need for dependencies among data in all of them. The solution is full distribution, providing a single logical view to objects anywhere, from anywhere. Users see a logical model of objects connected to objects, with **atomic transactions** and propagating methods, even though composite objects are split among multiple databases, each under separate administrative control, on multiple, heterogeneous platforms, operating systems, and **network protocols** . 32-bit address spaces are not sufficient for this level of integration, so Objectivity/DB is based on 64 bits, providing access to millions of tera-objects, each of which may be

many gigabytes. Support for production environments includes multiple schemas, which may be shared among databases or private, encrypted schemas, dynamic addition of schemas, and schema evolution. Integration must include legacy databases, such as RDBMSs, in this same transparent logical view of objects, and must cooperate with standards such as ODMG-93 and the OMG CORBA. Finally, the logical view must remain valid, and applications must continue to work, as the mapping to the physical environment changes, moving objects and databases to new platforms. (0 Refs)

Subfile: B C

Descriptors: client-server systems; object-oriented databases; protocols; standards

Identifiers: 64 bit distributed client-server computing; downsizing; manufacturing information systems; enterprise-wide modeling; operations optimization; **atomic transactions** ; operating systems; **network protocols** ; ODMG-93; OMG CORBA

Class Codes: B6150M (Protocols); C5640 (Protocols); C6160J (Object-oriented databases); C5620L (Local area networks)

13/5/63 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

4517593 INSPEC Abstract Number: B9312-6230Y-003

Title: Architecture and analysis of fast packet switches **based on time-multiplexed photonic fabrics**

Author(s): Aly, K.A.; Dowd, P.W.

Author Affiliation: Dept. of Electr. & Comput. Eng., State Univ. of New York, Buffalo, NY, USA

Journal: Journal of High Speed Networks vol.2, no.2 p.145-68

Publication Date: 1993 Country of Publication: Netherlands

CODEN: JHSNEB ISSN: 0926-6801

Language: English Document Type: Journal Paper (JP)

Treatment: Practical (P); Theoretical (T)

Abstract: This paper proposes and evaluates two fast **packet switching** architectures based on time-division multiplexed integrated photonic fabrics. The architectures are targeted towards low-latency **inter - node switching** and intra- **node** routing in high-speed **networks** . The **inter - node switch** achieves output **packet** queueing via asynchronous time-division multiplexing a strictly-nonblocking photonic fabric. Buffer behavior is analyzed at both input and output stages to determine the effect of varying the **switching** bandwidth on the performance metrics (delay, throughput, and **packet** loss probability). Analysis is performed for finite **switch** dimensions by obtaining upper and lower bounds on the **packet** loss at input. The dependence of finite output buffer latency and overflow probability on the normalized **switching** bandwidth is examined. The intra- **node** trunk traffic **router** consists of a passive optical coupler followed by an active routing stage. For this architecture, both synchronous and asynchronous time-division multiplexing modes are modeled and analyzed to obtain expressions for corresponding **packet** buffering delay and total **switching** latency. The **router** is shown to saturate at the waiting time singularity of its input (or output) buffers, given by the ratio of the **switching** bandwidth to the dimension. (36 Refs)

Subfile: B

Descriptors: optical communication equipment; optical **switches** ; **packet switching** ; queueing theory; telecommunication **network** routing; time division multiplexing

Identifiers: fast **packet switching** architectures; integrated photonic **switches** ; low-latency **inter - node switching** ; intra- **node** routing; high-speed **networks** ; output **packet** queueing; asynchronous time-division multiplexing; strictly-nonblocking photonic fabric; **switching** bandwidth; performance metrics; throughput; **packet** loss probability; finite output buffer latency; overflow probability; trunk traffic **router** ; passive optical coupler; active routing stage; synchronous time-division multiplexing; **packet** buffering delay; total **switching** latency; waiting time singularity; TDM

Class Codes: B6230Y (Other switching centres); B6260 (Optical links and equipment); B6150C (Switching theory); B6150J (Queueing systems)

13/5/76 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01819546 JICST ACCESSION NUMBER: 93A0701899 FILE SEGMENT: JICST-E
A Message **Communication** Network **for** Network **-wide Distributed Call Processing.**
TANAKA SATOSHI (1); MARUYAMA KATSUMI (1); KUBOTA MINORU (1)
(1) Nippon Telegraph & Telephone Corp.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1993, VOL.93,NO.160(SSE93 26-38), PAGE.55-60, FIG.7, REF.10
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.394/.395
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes an internode **message** communication and a **network** for **network** -wide distributed object-oeiented call processing with high speed and high capacity communication links. This method is supported to be applied for PLATINA, platform for telecommunication and **information network** applications. In PLATINA, **network** -wide distributed objects can communicate by **messages** . Low delay and high throughput are required for **message** communication facility. In an internode communication, an internode connection provides the reliable and effcient internode communication by multiplexing interobject **messages** . **Data messages** include confirmations of already received **messages** . In a **message** communication **network** , **message** transfer **nodes** that relay internode **messages** are connected to **switching nodes** . **Internode** connections between **switching nodes** and service control **nodes** are linked directly to reduce communication delay. (author abst.)
DESCRIPTORS: traffic processing; **message** transmission; distributed control; system **interface** ; **protocol** ; object oriented programming; throughput; public communication; communication repeating; signaling system; communication monitoring; digital communication
BROADER DESCRIPTORS: treatment; communication operation; operation(processing); communication system; method; control; **interface** ; rule; **computer** programming; performance; telecommunication; monitoring; communication administration; management
CLASSIFICATION CODE(S): ND11010T

13/5/80 (Item 3 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00811493 E94096099063
ATOMIC: a low-cost, very-high-speed, local communication architecture
(ATOMIC: Eine preiswerte, sehr schnelle, lokale Kommunikationsarchitektur)
Cohen, D; Finn, G; Feldermann, R; Schon, Ade
USC Marina del Rey, USA
Proc. of the 1993 Internat. Conf. on Parallel Processing, Vol. 1: Architecture, Syracuse, USA, Aug 16-20, 19931993
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8493-8983-6

ABSTRACT:
ATOMIC is an inexpensive O(gigabit) speed LAN built by USC/ISI. It is based upon Mosaic technology developed for fine-grain, message-passing, massively parallel computation. Each Mosaic processor is capable of routing variable

length packets, while providing added value through simultaneous computing and buffering. ATOMIC adds a general routing capability to the native Mosaic wormhole routing through store-and-forward. ATOMIC scales linearly, with a small interface cost. Each ATOMIC channel has a data carrying capacity of 500 Mb/s. A prototype ATOMIC LAN has been constructed along with **host interfaces** and software that provides full TCP/IP compatibility. Using **ATOMIC** , 1500 byte **packets** have been exchanged between hosts at an aggregate transfer rate of more than 1 Gb/s. Other tests have demonstrated throughput of 5.25 million packets per second over a single Mosaic channel. This paper describes the architecture and performance of ATOMIC.

DESCRIPTORS: LAN--LOCAL AREA NETWORKS; NETWORK ARCHITECTURE; NETWORK STUCTURE--ELECTRIC; PARALLEL PROCESSING; PACKET SWITCHING; SWITCHING TECHNOLOGY
IDENTIFIERS: lokales Netz; Parallelverarbeitung

```
Set     Items   Description
S1          0   (INTERNODE? OR INTER()NODE?)(2W)SWITCH?
S2      31243   SWITCH? OR INTERFACE? OR PROTOCOL? OR ADAPTER? OR CONTROL(-
             )DEVICE? OR ROUTER? OR BRIDGE? OR MULTIPLAYER?
S3      75510   NODE? OR CLIENT? OR STAND()ALONE? OR STANDALONE? OR PC OR -
            WORKSTATION? OR WORK()STATION? OR COMPUTER? OR NETWORK? OR LAN
             OR LANS OR INTRANET? OR PROCESSOR? OR HOST? OR SERVER? OR CPU
             OR MICROCOMPUTER?
S4      62687   MESSAGE? OR DATA OR INFORMATION OR TRANSACTION? OR PACKET?
            OR (E OR ELECTRONIC)()MAIL OR EMAIL OR TEXT
S5         11   ATOMIC (2N) S4
S6      16187   S2 AND S3 AND S4
S7          2   S6 AND S5
S8          1   S7 NOT PY>2001
S9          1   S8 NOT PD>20010426
File 256:SoftBase:Reviews,Companies&Prods. 82-2004/May
         (c)2004 Info.Sources Inc
```

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Set      Items   Description
S1           7   (INTERNODE? OR INTER()NODE?)(2W)SWITCH?
S2     1797691   SWITCH? OR INTERFACE? OR PROTOCOL? OR ADAPTER? OR CONTROL(-
              )DEVICE? OR ROUTER? OR BRIDGE? OR MULTIPLAYER?
S3     1917487   NODE? OR CLIENT? OR STAND()ALONE? OR STANDALONE? OR PC OR -
             WORKSTATION? OR WORK()STATION? OR COMPUTER? OR NETWORK? OR LAN
              OR LANS OR INTRANET? OR PROCESSOR? OR HOST? OR SERVER? OR CPU
              OR MICROCOMPUTER?
S4     3116357   MESSAGE? OR DATA OR INFORMATION OR TRANSACTION? OR PACKET?
             OR (E OR ELECTRONIC)()MAIL OR EMAIL OR TEXT
S5         229   ATOMIC (2N) S4
S6      285210   S2 AND S3 AND S4
S7           6   S6 AND S1
S8          21   S2 AND S3 AND S5
S9          27   S7 OR S8
S10         21   S9 AND IC=G06F?
S11          1   S9 AND MC=(T01-N01D OR T01-N02A3B)
S12         21   S10 OR S11
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
```

12/5/5 **(Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

015227752 **Image available**
WPI Acc No: 2003-288665/200328
XRPX Acc No: N03-229496
Multi- processor **system receives** messages **and transmits output to** nodes **that connect input** switches **following same ordering rule relative to input** switches **from which** messages **are received simultaneously**
Patent Assignee: SHARMA M (SHAR-I); STEELY S C (STEE-I); VAN DOREN S R (VDOR-I)
Inventor: SHARMA M; STEELY S C; VAN DOREN S R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020194290	A1	20021219	US 2001843228	A	20010426	200328	B

Priority Applications (No Type Date): US 2001843228 A 20010426
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020194290	A1		6	G06F-015/167	

Abstract (Basic): US 20020194290 A1
NOVELTY - The system includes a **switching** unit (12) having input **switches** (180-187) to receive **messages** from different **processors**, and to transmit **messages** to inter **switch** output terminals. Output **switches** (200-207) receive **messages** from the inter **switch** output terminals and transmit output to **nodes** (1000-1077) that connect the input **switches** following same ordering rule relative to the input **switches** from which the **messages** are received simultaneously.
USE - For inter- **processor** communication.
ADVANTAGE - Maintains **data** consistency in multi- **processor data** processing systems using **inter node switch**.
DESCRIPTION OF DRAWING(S) - The figure shows the multi- **processor** system.
Nodes (1000-1077)
Switching unit (12)
Input **switches** (180-187)
Output **switches** (200-207)
pp; 6 DwgNo 1/1
Title Terms: MULTI; **PROCESSOR**; SYSTEM; RECEIVE; **MESSAGE**; TRANSMIT; OUTPUT; **NODE**; CONNECT; INPUT; **SWITCH**; FOLLOW; ORDER; RULE; RELATIVE; INPUT; **SWITCH**; **MESSAGE**; RECEIVE; SIMULTANEOUS
Derwent Class: T01
International Patent Class (Main): **G06F-015/167**
File Segment: EPI

12/5/9 **(Item 6 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

012944958 **Image available**
WPI Acc No: 2000-116811/200010
XRPX Acc No: N00-088427
Access control management system in computer
Patent Assignee: OZ INTERACTIVE INC (OZIN-N); KEY-TRAK INC (KEYT-N)
Inventor: MALONEY W C; PORKELSSON H H
Number of Countries: 022 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9966429	A1	19991223	WO 99US13829	A	19990618	200010	B
AU 9946958	A	20000105	AU 9946958	A	19990618	200024	
US 20010004235	A1	20010621	US 9899954	A	19980911	200137	
			US 99392175	A	19990909		

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                              US 2001782070   A   20010212
US 20010006368  A1  20010705  US 9899954      A   19980911  200139
                              US 99393223     A   19990909
                              US 2001797338   A   20010301
US 20010009397  A1  20010726  US 9899954      A   19980911  200146
                              US 99393225     A   19990909
                              US 2001792987   A   20010226
Priority Applications (No Type Date): US 9899954 A 19980619; US 9899954 P
  19980911; US 99392175 A 19990909; US 2001782070 A 20010212; US 99393223 A
  19990909; US 2001797338 A 20010301; US 99393225 A 19990909; US 2001792987
  A 20010226
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
WO 9966429    A1 E  24 G06F-017/30
   Designated States (National): AU CA JP
   Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU
   MC NL PT SE
AU 9946958    A         G06F-017/30   Based on patent WO 9966429
US 20010004235 A1       G08B-013/14    Provisional application US 9899954

                                       Cont of application US 99392175
US 20010006368 A1       G08B-013/14    Provisional application US 9899954

                                       Cont of application US 99393223
                                       Cont of patent US 6204764
US 20010009397 A1       H04Q-001/00    Provisional application US 9899954

                                       Cont of application US 99393225
                                       Cont of patent US 6195005

Abstract (Basic): WO 9966429 A1
        NOVELTY - Various partitionable databases are distributed in
    multiple servers in hierarchical manner. Each client access the
    database, by connecting with respective top level sensors. The access
    is controlled such that database is accessed irrespective of access
    condition of other client .
        DETAILED DESCRIPTION - The link between the databases is
    established based on the key values stored in respective relational
    database. Network modifications are forwarded to the database via a
    distributed access control system and authenticated by servers .
    Database is forwarded through distributed atomic transaction
    interface . The database are distributed in hierarchical real time
    manner.
        USE - For database distribution management in computer network
    and for ATM network , LAN , internet.
        ADVANTAGE - Provision of hierarchical distributed database, results
    in simultaneous access by multiple users resulting in low access time.
        DESCRIPTION OF DRAWING(S) - The figure shows the representation of
    a key value pair in a relational database.
        pp; 24 DwgNo 2/8
Title Terms: ACCESS; CONTROL; MANAGEMENT; SYSTEM; COMPUTER
Derwent Class: T01
International Patent Class (Main): G06F-017/30 ; G08B-013/14; H04Q-001/00
File Segment: EPI


 12/5/11     (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004  Thomson Derwent. All rts. reserv.

012841116    **Image available**
WPI Acc No: 2000-012948/200001
XRPX Acc No: N00-010060
   Atomic  transaction  processing method in multi bus  computer  system
Patent Assignee: INTEL CORP (ITLC )
Inventor: CHITTOR S; KAPUR S; LOOI L
Number of Countries: 001  Number of Patents: 001
```

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5987552	A	19991116	US 9813774	A	19980126	200001	B

Priority Applications (No Type Date): US 9813774 A 19980126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5987552	A		12	G06F-013/00	

Abstract (Basic): US 5987552 A

NOVELTY - A **transaction** of **atomic** sequence is received and terminated on the local bus. The transaction is performed on the remote bus, and a response to the transaction is received and placed on the local bus.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for local bridging agent.

USE - In multi bus **computer** system to process sequence of **atomic transaction** .

ADVANTAGE - Improves utilization of the bus and provides lockout. **Protocol** has remote initiated lockouts that simulate remote agents uninterrupted access to an agent on the local bus.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of local bridging agent.

pp; 12 DwgNo 3/5

Title Terms: ATOMIC; TRANSACTION; PROCESS; METHOD; MULTI; BUS; **COMPUTER** ; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-013/00**
International Patent Class (Additional): **G06F-013/42**
File Segment: EPI

12/5/13 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011591243 **Image available**
WPI Acc No: 1998-008372/199801
XRPX Acc No: N98-006669

Computer **database method for database with** data **organised into** atomic data **sets - involves delaying execution of command if existing locks are found, and determining id deadlock exist, related projections are merged together and re-executed to recover from deadlock**

Patent Assignee: US SEC OF NAVY (USNA); US DEPT OF THE NAVY (USNA)
Inventor: FORTIER P J
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US N8238045	N	19950201	US 94238045	A	19940428	199801	B
US 5752026	A	19980512	US 94238045	A	19940428	199826	

Priority Applications (No Type Date): US 94238045 A 19940428
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US N8238045	N		27	G06F-000/00	
US 5752026	A		10	G06F-017/30	

Abstract (Basic): US N8238045 N

The method involves organising the **data** into **atomic data** sets and separating transactions into projections which operate on only one **atomic data** set. Multiple transactions can then access the same **atomic data** set using a locking **protocol** where locks are held by each projection. On access to a data item, the system detects existing locks.

If locks are not found, the system locks the data and performs the access. When existing locks are found the system delays execution of the command and determines if a deadlock is present. To recover from a deadlock, related projections are merged together and re-executed. The

system merges related projections from other transactions and re-executes if the deadlock continues. When the deadlock continues after execution of the above steps, victim projection is chosen and aborted. The victim projection is restarted after commit of the conflicting projection.

ADVANTAGE - Provides early database commit while increasing database concurrency, and limits cascading aborts to minimise impact on recovery for decomposed database and transaction system.

Dwg.4/4

US 8238045 N

The method involves organising the **data** into **atomic data** sets and separating transactions into projections which operate on only one **atomic data** set. Multiple transactions can then access the same **atomic data** set using a locking **protocol** where locks are held by each projection. On access to a data item, the system detects existing locks.

If locks are not found, the system locks the data and performs the access. When existing locks are found the system delays execution of the command and determines if a deadlock is present. To recover from a deadlock, related projections are merged together and re-executed. The system merges related projections from other transactions and re-executes if the deadlock continues. When the deadlock continues after execution of the above steps, victim projection is chosen and aborted. The victim projection is restarted after commit of the conflicting projection.

ADVANTAGE - Provides early database commit while increasing database concurrency, and limits cascading aborts to minimise impact on recovery for decomposed database and transaction system.

Dwg.4/4

US 8238045 A

The method involves organising the **data** into **atomic data** sets and separating transactions into projections which operate on only one **atomic data** set. Multiple transactions can then access the same **atomic data** set using a locking **protocol** where locks are held by each projection. On access to a data item, the system detects existing locks.

If locks are not found, the system locks the data and performs the access. When existing locks are found the system delays execution of the command and determines if a deadlock is present. To recover from a deadlock, related projections are merged together and re-executed. The system merges related projections from other transactions and re-executes if the deadlock continues. When the deadlock continues after execution of the above steps, victim projection is chosen and aborted. The victim projection is restarted after commit of the conflicting projection.

ADVANTAGE - Provides early database commit while increasing database concurrency, and limits cascading aborts to minimise impact on recovery for decomposed database and transaction system.

Dwg.4/4

Title Terms: **COMPUTER** ; DATABASE; METHOD; DATABASE; DATA; ORGANISE; ATOMIC ; DATA; SET; DELAY; EXECUTE; COMMAND; EXIST; LOCK; FOUND; DETERMINE; ID; DEADLOCK; EXIST; RELATED; PROJECT; MERGE; EXECUTE; RECOVER; DEADLOCK

Derwent Class: T01

International Patent Class (Main): **G06F-000/00 ; G06F-017/30**

International Patent Class (Additional): **G06F-017/60**

File Segment: EPI

12/5/15 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011164361 **Image available**

WPI Acc No: 1997-142286/199713

XRPX Acc No: N97-117808

Distributed transaction processing system e.g. for computer **- processes object inclination transaction and taken type transaction and**

co-ordinating them so that transaction result depends on results of both of them

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: FREUND T J; HOLDSWORTH S A J; SMITH S A
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9022356	A	19970121	JP 95316943	A	19951205	199713	B
US 6138169	A	20001024	US 94355870	A	19941214	200055	
			US 97840999	A	19970422		

Priority Applications (No Type Date): US 94355870 A 19941214; US 97840999 A 19970422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9022356	A		19	G06F-009/44	
US 6138169	A			G06F-015/163	Cont of application US 94355870

Abstract (Basic): JP 9022356 A

The system performs an object inclination transaction when an object inclination transaction request is received through two or more programming **interfaces** of a first co-ordinator of necessary procedure. Then, the results of processing are returned. Similarly, a transaction processing of a taken type transaction is performed, when a corresponding request is received. Then results of processing are returned.

The results of both processing are co-ordinated, to form a single **atomic transaction** so that an object inclination calling method is converted into a taken type call of the necessary procedure using an implementation class. The implementation class also accepts the up call from taken type TRAN of the necessary procedure and converts it to a required object transaction service calling method.

ADVANTAGE - Attains transaction processing which combines independent type and distributed type transaction processing.

Dwg.2/8

Title Terms: DISTRIBUTE; TRANSACTION; PROCESS; SYSTEM; **COMPUTER** ; PROCESS; OBJECT; INCLINATION; TRANSACTION; TYPE; TRANSACTION; CO; ORDINATE; SO; TRANSACTION; RESULT; DEPEND; RESULT
Derwent Class: T01
International Patent Class (Main): **G06F-009/44** ; **G06F-015/163**
File Segment: EPI

12/5/17 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011021246 **Image available**
WPI Acc No: 1996-518196/199651
Related WPI Acc No: 1997-297646
XRPX Acc No: N96-436713

Atom and ion computer **modelling system - performs atomic computations to calculate and construct mathematical atomic models based on specific** atomic data **which is input by operator and retrieved from stored atomic database**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: MOHANTY A K; PARPIA F A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5574844	A	19961112	US 94310459	A	19940922	199651	B

Priority Applications (No Type Date): US 94310459 A 19940922
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5574844	A		15	G06F-015/00	

Abstract (Basic): US 5574844 A

The **computer** includes a data processing system, a visual display unit and a data entry device. An operating system, a text-graphic interactive user **interface** and a number of atomic structure programs reside in the data processing system. The atomic structure programs perform atomic computations to calculate and construct mathematical atomic models based on specific **atomic data** which is input by an operator and retrieved from a stored **atomic data** base.

The text-graphic interactive user **interface** includes the following programs: SMARTPET (SMART PEriodic Table tool), ATOMGRAF (ATOMic GRAph(F)ics), RASPIE (Relativistic Atomic Structure Program Interactive Environment), and ATOMBAS (**ATOMic data** BASe). SMARTPET presents **atomic data** in familiar formats so that a user can select and identify the atom or ion to be investigated. RASPIE provides a windows-based interactive environment for communication between the user and the atomic structure programs. RASPIE furnishes the input-output (I-O) requirements of atomic structure programs. ATOMGRAF generates graphical quantitative plots of the output results of atomic structure programs. ATOMBAS is a data base storing information for the construction of atomic models for basis set programs.

ADVANTAGE - **Computer** technique for providing user-friendly environment which simplifies construction of relativistic models of atoms and ions.

Dwg.1/10

Title Terms: ATOM; ION; **COMPUTER** ; MODEL; SYSTEM; PERFORMANCE; ATOMIC; COMPUTATION; CALCULATE; CONSTRUCTION; MATHEMATICAL; ATOMIC; MODEL; BASED; SPECIFIC; ATOMIC; DATA; INPUT; OPERATE; RETRIEVAL; STORAGE; ATOMIC; DATABASE

Derwent Class: T01

International Patent Class (Main): **G06F-015/00**

File Segment: EPI

12/5/18 (Item 15 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010620236 **Image available**

WPI Acc No: 1996-117189/199612

XRPX Acc No: N96-097928

Semaphore communication method between incompatible bus locking architectures - uses atomic transactions **supported by bus** protocols **of each bus to implement semaphore to establish exclusive access transactions between source and destination** nodes **located on source and destination buses**

Patent Assignee: APPLE COMPUTER INC (APPY)

Inventor: KREIN W T

Number of Countries: 056 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9603697	A1	19960208	WO 95US9313	A	19950720	199612 B
AU 9531433	A	19960222	AU 9531433	A	19950720	199621

Priority Applications (No Type Date): US 94278274 A 19940721

Cited Patents: EP 366432; EP 492817; US 5379384

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9603697	A1	E	24	G06F-013/40	

Designated States (National): AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE KG KP MD MG MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TT UA UG UZ VN

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT KE LU MC MW NL OA PT SD SE SZ UG

AU 9531433 A G06F-013/40 Based on patent WO 9603697

Abstract (Basic): WO 9603697 A

The semaphore method establishes exclusive transactions between

source and destination **nodes** in a multiple bus **computer** system, and involves selecting an automatic transaction for each bus **protocol** to mediate exclusive access transactions involving the corresp bus, and using **bridges** which couple different pairs of buses to monitor the buses for the selected **atomic transactions** . A source **node** on one bus initiates an exclusive access transaction to a destination **node** by launching the selected **atomic transaction** appropriate for the source bus to the destination **node** .

When the path between the source and destination **nodes** requires transit of more than one bus, each **bridge** that couples a pair of buses in the path detects an outgoing **atomic transaction** appropriate for the other bus to the destination **node** .

USE/ADVANTAGE - **Computer** implemented method for granting source **node** on first bus exclusive access to destination **node** on second bus coupled to first bus. Provides exclusive access to shared resources without reducing bandwidth of buses.

Dwg.1/5

Title Terms: SEMAPHORE; COMMUNICATE; METHOD; INCOMPATIBLE; BUS; LOCK; ATOMIC; TRANSACTION; SUPPORT; BUS; BUS; IMPLEMENT; SEMAPHORE; ESTABLISH; EXCLUDE; ACCESS; TRANSACTION; SOURCE; DESTINATION; **NODE** ; LOCATE; SOURCE ; DESTINATION; BUS

Derwent Class: T01

International Patent Class (Main): **G06F-013/40**

File Segment: EPI

12/5/19 (Item 16 from file: 350)

007161705

WPI Acc No: 1987-158714/198723

XRPX Acc No: N87-119131

Multi- node data **processing system - has non-active** inter - node switch **configured to route** messages **from local** processor **to active** switch

Patent Assignee: INT COMPUTERS LTD (INCM)

Inventor: DUXBURY C M; YATES R

Number of Countries: 008 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 225022	A	19870610	EP 86307965	A	19861015	198723	B
ZA 8607907	A	19870421				198727	
AU 8665569	A	19870528				198728	
US 4773067	A	19880920	US 86921211	A	19861020	198840	
EP 225022	B	19911113				199146	
DE 3682486	G	19911219				199201	

Priority Applications (No Type Date): GB 8528892 A 19851123

Cited Patents: 1.Jnl.Ref; A3...8926; DE 2007041; No-SR.Pub; US 4550397; WO 8203739

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 225022	A	E	19		
Designated States (Regional): DE FR GB IT NL					
US 4773067	A		17		
EP 225022	B				
Designated States (Regional): DE FR GB IT NL					

Abstract (Basic): EP 225022 A

The system includes a number of **data** processing **nodes** (10-13) each including a **data** processing unit (PROC) and a **switching** unit (INS). In operation the **switching** unit in any one of the **nodes** can be selected to act as a star coupler for receiving **messages** from any of the **nodes** and broadcasting each **message** to all the **nodes** . The **switching** unit in each other **node** acts to relay **messages** between the processing unit in that **node** and the selected **switching** unit.

The **switching** units in all the **nodes** are pref. identical in structure and each pref. includes a configuration register which can be selectively set to indicate which of the **switching** units is currently to act as the star coupler.

ADVANTAGE - Avoids problems of prior art systems having a central star coupler, failure of which resulting in the **nodes** being unable to communicate. In the present system, if one **switch** fails, another may be designated as a star coupler. **Switching** units are connected together by means of optical fibres.

1/14

Title Terms: MULTI; **NODE** ; **DATA** ; PROCESS; SYSTEM; NON; ACTIVE; INTER; **NODE** ; **SWITCH** ; CONFIGURATION; ROUTE; **MESSAGE** ; LOCAL; **PROCESSOR** ; ACTIVE; **SWITCH**
Derwent Class: T01; W01
International Patent Class (Additional): **G06F-015/16** ; H04J-003/26
File Segment: EPI

12/5/20 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007130472
WPI Acc No: 1987-130469/198719
XRPX Acc No: N87-097590

Re-startable data base system switch **-over method - having backup** processor **performing necessary recovery processing and taking over user-transaction processing when active** processor **fails**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: FUKUMOTO T; FUNAHASHI T; SCHWEIKERT G; SCOFIELD H; WALKER T E; YOUNG J W; WALKER T; YOUNG J; SCHIVEIKERT G
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 221274	A	19870513	EP 86111955	A	19860829	198719	B
EP 221274	B1	19920701	EP 86111955	A	19860829	199227	
DE 3685870	G	19920806	DE 3685870	A	19860829	199233	
			EP 86111955	A	19860829		
US 5155678	A	19921013	US 85792371	A	19851029	199244	

Priority Applications (No Type Date): US 85792371 A 19851029
Cited Patents: 4.Jnl.Ref; A3...8910; No-SR.Pub; GB 1163859
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 221274	A	E	27		
	Designated States (Regional): DE FR GB IT				
EP 221274	B1	E	29	G06F-011/20	
	Designated States (Regional): DE FR GB IT				
DE 3685870	G			G06F-011/20	Based on patent EP 221274
US 5155678	A		23	G06F-011/08	

Abstract (Basic): EP 221274 A

The method for ensuring **switch** over in a restartable data base system between a backup and a degrading active **processor** comprises the steps of establishing a session between the terminal accessing the active **processor** with **atomic transactions** and the active **processor** . Active **processor** unavailability is prepared for by synchronising with, tracking, and monitoring the active **processor** 's log entries by the backup **processor** .

In the event of active **processor** unavailability, recovery processing is performed by the backup **processor** including taking over transaction processing as the new active **processor** .

ADVANTAGE - Maximises transaction integrity and consistency

Title Terms: DATA; BASE; SYSTEM; **SWITCH** ; METHOD; **PROCESSOR** ; PERFORMANCE ; NECESSARY; RECOVER; PROCESS; USER; TRANSACTION; PROCESS; ACTIVE; **PROCESSOR** ; FAIL
Derwent Class: T01

International Patent Class (Main): **G06F-011/08 ; G06F-011/20**
File Segment: EPI

```
Set     Items   Description
S1         62   AU='STEELY S':AU='STEELY SIMON CARL JR'
S2        126   AU='SHARMA M' OR AU='SHARMA MADHUMITRA'
S3         46   AU='VAN DOREN S' OR AU='VAN DOREN S R' OR AU='VAN DOREN ST-
               EPHEN R'
S4         14   AU='VANDOREN S R' OR AU='VANDOREN STEPHEN R'
S5        195   S1 OR S2 OR S3 OR S4
S6        113   S5 AND IC=G06F?
S7         20   S6 AND IC=G06F-015?
File 347:JAPIO Nov 1976-2004/Jan(Updated 040506)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Jun W01
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040603,UT=20040527
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200435
         (c) 2004  Thomson Derwent
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7/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06341217 **Image available**
LOW OCCUPANCY PROTOCOL FOR MANAGING SIMULTANEOUS TRANSACTIONS WITH DEPENDENCY

PUB. NO.: 11-282821 [JP 11282821 A]
PUBLISHED: October 15, 1999 (19991015)
INVENTOR(s): **STEELY SIMON C**
SHARMA MADHUMITRA
VANDOREN STEPHEN R
APPLICANT(s): DIGITAL EQUIP CORP <DEC>
APPL. NO.: 10-340925 [JP 98340925]
FILED: October 26, 1998 (19981026)
PRIORITY: 957565 [US 957565], US (United States of America), October 24, 1997 (19971024)
INTL CLASS: **G06F-015/177 ; G06F-012/08 ; G06F-012/08 ; G06F-015/16 ; G06F-015/167**

ABSTRACT

PROBLEM TO BE SOLVED: To provide an SMP (symmetrical multiprocessor system) where many multiprocessor nodes including shared memories are connected to each other via a switch.

SOLUTION: Each of architecture and coherence protocol which are used to a large SMP has a hierarchy switch structure to connect many multiprocessor nodes 10 to a switch 15 and to make them operate with each optimum performance. Every node 10 has a simultaneous buffer system to enable all processors of the node to operate with its optimum performance and also includes many elements, i.e., a victim cache, a directory and a transaction tracking table to maintain the memory coherence. The victim cache selectively selects the victim data having a preceding remote node memory to improve all performance of the memory. A delay writing buffer which is used with the directory and identifies the victim written in the memory improves better the memory performance.

7/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06341216 **Image available**
SEQUENCE SUPPORT MECHANISM FOR MULTIPROCESSOR SYSTEM USING SWITCH AS ITS BASE

PUB. NO.: 11-282820 [JP 11282820 A]
PUBLISHED: October 15, 1999 (19991015)
INVENTOR(s): **VANDOREN STEPHEN R**
STEELY SIMON C
SHARMA MADHUMITRA
FENWICK DAVID M
APPLICANT(s): DIGITAL EQUIP CORP <DEC>
APPL. NO.: 10-340924 [JP 98340924]
FILED: October 26, 1998 (19981026)
PRIORITY: 957298 [US 957298], US (United States of America), October 24, 1997 (19971024)
INTL CLASS: **G06F-015/177 ; G06F-015/177 ; G06F-012/08 ; G06F-015/16 ; G06F-015/167**

ABSTRACT

PROBLEM TO BE SOLVED: To provide an SMP (symmetrical multiprocessor system)

where many multiprocessor nodes including shared memories are connected to each other via a switch.

SOLUTION: Each of architecture and coherence protocol which are used to a large SMP has a hierarchy switch structure to connect many multiprocessor nodes 10 to a switch 15 and to make them operate with each optimum performance. Every node 10 has a buffer system to enable all processors of the node to operate with its optimum performance and also includes many elements, i.e., a victim cache, a directory and a transaction tracking table to maintain the memory coherence. An arbitration bus which is connected to the output side of the directory gives the center sequencing points to all messages that are sent via the SMP. Using a virtual channel can maintain the data coherence by means of a simple method that maintains the system sequence.

7/5/3 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00738306
System bus with separate address and data bus protocols
Systembus mit getrennten Protokollen fur Adresse und Databus
Bus systeme avec protocoles separes de bus d'adresses et de donnees
PATENT ASSIGNEE:
DIGITAL EQUIPMENT CORPORATION, (313089), 111 Powdermill Road, Maynard, Massachusetts 01754-1499, (US), (applicant designated states: DE;FR;GB;IT;NL)
INVENTOR:
Fenwick, David M., 6 Pennsylvania Avenue, Chelmsford, Massachusetts 01824, (US)
van Doren, Stephen R. , 237 South Street, No. 5, Shrewsbury, Massachusetts 01545, (US)
Foley, Denis J., 88 Lamplighter Drive, Shrewsbury, Massachusetts 01545, (US)
Keck, Dale R., 4 Wiltshire Drive, Shrewsbury, Massachusetts 01545, (US
LEGAL REPRESENTATIVE:
Charig, Raymond Julian et al (79692), Eric Potter Clarkson, Park View House, 58 The Ropewalk, Nottingham NG1 5DD, (GB)
PATENT (CC, No, Kind, Date): EP 695999 A2 960207 (Basic)
EP 695999 A3 980708
APPLICATION (CC, No, Date): EP 95304598 950629;
PRIORITY (CC, No, Date): US 269222 940630
DESIGNATED STATES: DE; FR; GB; IT; NL
INTERNATIONAL PATENT CLASS: **G06F-013/42** ; **G06F-015/16**

ABSTRACT EP 695999 A2
Bus interfaces for nodes coupled to a system bus in a computer system, the system bus including an address bus and a separate data bus. System bus operations include address and command transactions and data transactions. Data transactions occur on the data bus separately and independently of the occurrence of address and command transactions on the address bus. A bus interface may include any of a commander address bus interface means for providing to an address bus address and command transactions, a responder address bus interface means for acknowledging receipt of address and command transactions via the address bus, a commander data bus interface means for controlling submission to the data bus of data transactions as a result of the occurrence of address and command transactions on the address bus, and a responder data bus interface means for transferring data on the data bus during a data transaction. Data transactions occur on the data bus separately and independently of the occurrence of address and command transactions on the address bus. In particular, the timing of data transactions and the rate at which data transactions occur on the data bus is independent of the timing of address and command transactions and the rate at which

address sub-transactions occur on the address bus. (see image in original document)
ABSTRACT WORD COUNT: 248

LEGAL STATUS (Type, Pub Date, Kind, Text):

Assignee:	000531	A2	Transfer of rights to new applicant: Compaq Computer Corporation (687792) 20555 S.H. 249 Houston Texas 77070 US
Application:	960207	A2	Published application (A1with Search Report ;A2without Search Report)
Change:	040602	A2	Legal representative(s) changed 20040414
Examination:	040121	A2	Date of dispatch of the first examination report: 20031204
Search Report:	980708	A3	Separate publication of the European or International search report
Change:	980708	A2	Obligatory supplementary classification (change)
Examination:	990224	A2	Date of filing of request for examination: 981218

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	758
SPEC A	(English)	EPAB96	16334
Total word count - document A			17092
Total word count - document B			0
Total word count - documents A + B			17092

7/5/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015838513 **Image available**
WPI Acc No: 2003-900717/200382
XRPX Acc No: N03-719096

Test pattern quality determination apparatus for integrated circuits, determines delay defect exposure quality metric associated with test pattern, to indicate defect exposure capability of test pattern

Patent Assignee: REARICK J (REAR-I); SHARMA M (SHAR-I); AGILENT TECHNOLOGIES INC (AGIL-N)
Inventor: REARICK J; **SHARMA M**
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030204350	A1	20031030	US 2002137534	A	20020430	200382	B
US 6708139	B2	20040316	US 2002137534	A	20020430	200420	

Priority Applications (No Type Date): US 2002137534 A 20020430
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030204350	A1		19	G06F-019/00	
US 6708139	B2			G06F-015/00	

Abstract (Basic): US 20030204350 A1

NOVELTY - A logic circuit determines a delay corresponding to the longest sensitizable path of integrated circuit model, and a delay associated with actual path exercised by the test pattern. A delay defect exposure (DDE) quality metric associated with the pattern is determined based on the delays, to indicate defect exposure capability of the test pattern.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) test pattern quality determination method; and

(2) integrated circuit testing program.

USE - For determining quality of test patterns used for testing integrated circuits.

ADVANTAGE - By determining quality metric for each test pattern, a

suitable test pattern for testing the fault site can be easily selected and implemented to ensure desired testing efficiency.

DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating the test pattern quality determination process.

pp; 19 DwgNo 6/8

Title Terms: TEST; PATTERN; QUALITY; DETERMINE; APPARATUS; INTEGRATE; CIRCUIT; DETERMINE; DELAY; DEFECT; EXPOSE; QUALITY; METRIC; ASSOCIATE; TEST; PATTERN; INDICATE; DEFECT; EXPOSE; CAPABLE; TEST; PATTERN

Derwent Class: S01; T01; U11

International Patent Class (Main): **G06F-015/00 ; G06F-019/00**

File Segment: EPI

7/5/5 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015523234 **Image available**

WPI Acc No: 2003-585381/200355

XRPX Acc No: N03-466010

Plain text printing control method, involves receiving keys from sources through secured and non-secured communication channel, and decrypting encrypted text document and printing it plain text document using keys

Patent Assignee: PITNEY BOWES INC (PITB)

Inventor: **SHARMA M**

Number of Countries: 097 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030081247	A1	20030501	US 200122462	A	20011030	200355	B
WO 200338677	A1	20030508	WO 2002US33792	A	20021021	200355	

Priority Applications (No Type Date): US 200122462 A 20011030

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030081247	A1		8	B41J-001/00	
WO 200338677	A1	E		G06F-017/30	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20030081247 A1

NOVELTY - The method involves receiving two keys from sources at a printer through a secure and non-secure electronic communication channels, and an encrypted version of plain text document from the source through the non-secure channel. Using the keys the encrypted document is decrypted to obtain a plain text document at the printer and a predetermined number of encrypted pages is printed at the printer port.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a system for securely transmitting and printing documents.

USE - Used for controlling the printing of a plain text document in electronic communication system.

ADVANTAGE - The method provides a separate password to each user, thereby prevents the third party to enter into others login. The data is decrypted only at the printing port thus if anyone access others document they cannot not view the content of it, thereby provides a very robust and secure document viewing method.

DESCRIPTION OF DRAWING(S) - The drawing shows flowchart showing the operation of the secure electronic document transfer system.

pp; 8 DwgNo 3/5

Title Terms: PLAIN; TEXT; PRINT; CONTROL; METHOD; RECEIVE; KEY; SOURCE; THROUGH; SECURE; NON; SECURE; COMMUNICATE; CHANNEL; ENCRYPTION; TEXT; DOCUMENT; PRINT; PLAIN; TEXT; DOCUMENT; KEY

Derwent Class: P75; S06; T01; T04; W01

International Patent Class (Main): B41J-001/00; **G06F-017/30**
International Patent Class (Additional): **G06F-015/00**
File Segment: EPI; EngPI

7/5/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015494318
WPI Acc No: 2003-556465/200352
XRPX Acc No: N03-442100
Novel variety of spray rose plant, named Olijdum, which abundantly forms attractive dark red double blossoms in form of very uniform spray, useful for producing cut floral sprays under greenhouse growing conditions
Patent Assignee: HEWLETT-PACKARD CO (HEWP); SHARMA M (SHAR-I)
Inventor: **SHARMA M**
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030081254	A1	20030501	US 2001984073	A	20011026	200352	B
JP 2003202975	A	20030718	JP 2002309141	A	20021024	200356	

Priority Applications (No Type Date): US 2001984073 A 20011026
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030081254	A1		13	B41J-001/00	
JP 2003202975	A		15	G06F-003/12	

Abstract (Basic): US 20030081254 A1
NOVELTY - A new and distinct variety of spray rose plant (I), named Olijdum, or its part, that forms in abundance attractive globular buds in the form of a very uniform spray, forms in abundance attractive dark red double blossoms, forms attractive semi-glossy light green foliage, and exhibits an erect growth habit, is new.
USE - (I) is useful in horticultural industry, for production of cut floral sprays under greenhouse growing conditions.
ADVANTAGE - (I) forms in abundance attractive globular buds in the form of a very uniform spray, forms in abundance attractive dark red double blossoms, forms attractive semi-glossy light green foliage, exhibits an erect growth habit, shows strong vegetation, abundant blooming, and exhibits very good resistance to diseases such as Botrytis and Mildew.
pp; 13 DwgNo 0/16
Title Terms: NOVEL; VARIETY; SPRAY; ROSE; PLANT; NAME; FORM; ATTRACT; DARK; RED; DOUBLE; BLOSSOM; FORM; UNIFORM; SPRAY; USEFUL; PRODUCE; CUT; FLORAL; SPRAY; GREENHOUSE; GROW; CONDITION
Derwent Class: P13; P75
International Patent Class (Main): B41J-001/00; **G06F-003/12**
International Patent Class (Additional): B41J-021/00; **G06F-015/00** ; H04N-001/00
File Segment: EngPI

7/5/7 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015319777 **Image available**
WPI Acc No: 2003-380712/200336
XRPX Acc No: N03-304098
Fault isolation method for network access server, involves allocation of modems to debug modem pool and session modem pool and initiating fault isolation or normal sessions based on predefined fault isolation criteria
Patent Assignee: CISCO TECHNOLOGY INC (CISC-N)
Inventor: **SHARMA M**
Number of Countries: 001 Number of Patents: 001

Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030041153 A1 20030227 US 2001938336 A 20010823 200336 B

Priority Applications (No Type Date): US 2001938336 A 20010823
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030041153 A1 6 G06F-015/16

Abstract (Basic): US 20030041153 A1

NOVELTY - The method involves allocating one or more modems associated with access server to debug modem pool and remaining modems to session modem pool. Incoming call to server is checked for predefined fault isolation criteria. If criteria are met, modem from debug modem pool is allocated and fault isolation session is initiated, else modem from session modem pool is allocated and normal session proceeds.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for an apparatus for fault isolating communication problems at a network access server.

USE - Used for fault isolation in network access server.

ADVANTAGE - The method selectively invokes fault isolation and hence fault isolation and problem solving are rendered compatible with the continued provision of highest possible level of normal client service with minimal impact.

DESCRIPTION OF DRAWING(S) - The drawing shows the flowchart illustrating the modem debug method for fault isolation.

pp; 6 DwgNo 2/2

Title Terms: FAULT; ISOLATE; METHOD; NETWORK; ACCESS; SERVE; ALLOCATE; MODEM; DEBUG; MODEM; POOL; SESSION; MODEM; POOL; INITIATE; FAULT; ISOLATE ; NORMAL; SESSION; BASED; PREDEFINED; FAULT; ISOLATE; CRITERIA
Derwent Class: T01; W01
International Patent Class (Main): **G06F-015/16**
International Patent Class (Additional): **G06F-015/173** ; H02H-003/05
File Segment: EPI

7/5/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015271212 **Image available**
WPI Acc No: 2003-332141/200331
XRPX Acc No: N03-266188

Broadband service provision method for plain old telephone system, involves receiving temporary dynamic internet protocol address in response to authentication request

Patent Assignee: SENAPATI A S (SENA-I); SHARMA M (SHAR-I)
Inventor: SENAPATI A S; **SHARMA M**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20030041151 A1 20030227 US 2001929321 A 20010814 200331 B

Priority Applications (No Type Date): US 2001929321 A 20010814
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20030041151 A1 18 G06F-015/16

Abstract (Basic): US 20030041151 A1

NOVELTY - An authentication request is transmitted from a modem to a single configuration domain name associated with broadband service node (BSN) through a point-to-point protocol over Ethernet (Pope) network. The temporary dynamic internet protocol (IP) address is received in response to the request.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) broadband service provision system; and
(2) computer program product for providing broadband service.
USE - For providing broadband service such as digital subscriber line (DSL) service in point-to-point over Ethernet (Pope) network, for plain old telephone system (POTS).
ADVANTAGE - Requires entry of domain in addition to user name during authentication phase without requiring user to input the domain name in addition to user's telephone number, thereby ensuring optimal operation. Reduces amount of information which are to be inputted manually during authentication, thereby reducing number of customer calls for technical support.
DESCRIPTION OF DRAWING(S) - The figure shows a flowchart illustrating broadband service provision process.
pp; 18 DwgNo 4A/6
Title Terms: BROADBAND; SERVICE; PROVISION; METHOD; PLAIN; TELEPHONE; SYSTEM; RECEIVE; TEMPORARY; DYNAMIC; PROTOCOL; ADDRESS; RESPOND; AUTHENTICITY; REQUEST
Derwent Class: T01; W01
International Patent Class (Main): **G06F-015/16**
International Patent Class (Additional): **G06F-015/177**
File Segment: EPI

7/5/9 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015251620 **Image available**
WPI Acc No: 2003-312546/200330
XRPX Acc No: N03-248954
Load locked execution method for multiprocessor computer, involves waiting for specific time before ownership of memory block is surrendered on receipt of ownership request, when invalidate messages are received by processor
Patent Assignee: SHARMA M (SHAR-I); STEELY S C (STEE-I); VAN DOREN S R (VDOR-I)
Inventor: **SHARMA M ; STEELY S C ; VAN DOREN S R**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030037223	A1	20030220	US 2001933536	A	20010820	200330	B

Priority Applications (No Type Date): US 2001933536 A 20010820
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030037223	A1		17	G06F-015/00	

Abstract (Basic): US 20030037223 A1
NOVELTY - A lock flag is reset on receipt of invalidate message for cache copy of memory block. When invalidate messages are received by a processor, the processor waits for a selected time interval before the ownership of the memory block is surrendered on receipt of ownership request message. The stored conditional instruction is executed by the processor to read the information from memory block, when lock flag is set.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) computer;
(2) multiprocessor computer operating method;
(3) multiprocessor computer system;
(4) computer readable medium storing multiprocessor computer operating program; and
(5) electromagnetic signals.
USE - For multiprocessor computer system (claimed).
ADVANTAGE - Reduces number of system commands and system overhead during contention for memory block. Avoids livelock by waiting for a predetermined period before surrendering ownership of memory block.

DESCRIPTION OF DRAWING(S) - The figure shows the transaction diagram during execution of load locked instruction.
pp; 17 DwgNo 2A/6
Title Terms: LOAD; LOCK; EXECUTE; METHOD; MULTIPROCESSOR; COMPUTER; WAIT; SPECIFIC; TIME; MEMORY; BLOCK; RECEIPT; REQUEST; INVALID; MESSAGE; RECEIVE; PROCESSOR
Derwent Class: T01
International Patent Class (Main): **G06F-015/00**
File Segment: EPI

7/5/10 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015227752 **Image available**
WPI Acc No: 2003-288665/200328
XRPX Acc No: N03-229496

Multi-processor system receives messages and transmits output to nodes that connect input switches following same ordering rule relative to input switches from which messages are received simultaneously

Patent Assignee: SHARMA M (SHAR-I); STEELY S C (STEE-I); VAN DOREN S R (VDOR-I)
Inventor: **SHARMA M ; STEELY S C ; VAN DOREN S R**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020194290	A1	20021219	US 2001843228	A	20010426	200328	B

Priority Applications (No Type Date): US 2001843228 A 20010426
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020194290	A1		6	G06F-015/167	

Abstract (Basic): US 20020194290 A1
NOVELTY - The system includes a switching unit (12) having input switches (180-187) to receive messages from different processors, and to transmit messages to inter switch output terminals. Output switches (200-207) receive messages from the inter switch output terminals and transmit output to nodes (1000-1077) that connect the input switches following same ordering rule relative to the input switches from which the messages are received simultaneously.
USE - For inter-processor communication.
ADVANTAGE - Maintains data consistency in multi-processor data processing systems using inter node switch.
DESCRIPTION OF DRAWING(S) - The figure shows the multi-processor system.
Nodes (1000-1077)
Switching unit (12)
Input switches (180-187)
Output switches (200-207)
pp; 6 DwgNo 1/1
Title Terms: MULTI; PROCESSOR; SYSTEM; RECEIVE; MESSAGE; TRANSMIT; OUTPUT; NODE; CONNECT; INPUT; SWITCH; FOLLOW; ORDER; RULE; RELATIVE; INPUT; SWITCH; MESSAGE; RECEIVE; SIMULTANEOUS
Derwent Class: T01
International Patent Class (Main): **G06F-015/167**
File Segment: EPI

7/5/11 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014877060 **Image available**
WPI Acc No: 2002-697766/200275
XRPX Acc No: N02-550227

Cache coherency mechanism operating method for distributed computer system, involves encoding network routing information into sectored presence bits which are organized as arbitration masks

Patent Assignee: DOREN S V (DORE-I); SHARMA M (SHAR-I); STEELY S C (STEE-I)
Inventor: DOREN S V; **SHARMA M ; STEELY S C**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020099833	A1	20020725	US 2001768418	A	20010124	200275 B

Priority Applications (No Type Date): US 2001768418 A 20010124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020099833	A1		10	G06F-013/00	

Abstract (Basic): US 20020099833 A1

NOVELTY - The network routing information is encoded into sectored presence bits which are organized as arbitration masks. An invalidate message that includes the masks is produced at the home mode, when the data of interest is the subject of an update operation. The invalidate message is routed over the paths indicated by the decoded information of the applicable masks to the processors.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for distributed computer system.

USE - For operating cache coherency mechanism for distributed shared memory computer system (claimed) such as symmetric multiprocessor system.

ADVANTAGE - Masks allows the switching devices to determine the routes for the multicast transmission without the need for entering the larger network routing tables and thus without the associated delays.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of a cache coherency directory.

pp; 10 DwgNo 2/6

Title Terms: CACHE; COHERE; MECHANISM; OPERATE; METHOD; DISTRIBUTE; COMPUTER; SYSTEM; ENCODE; NETWORK; ROUTE; INFORMATION; SECTOR; PRESENCE; BIT; ORGANISE; ARBITER; MASK
Derwent Class: T01; W01
International Patent Class (Main): **G06F-013/00**
International Patent Class (Additional): **G06F-012/00 ; G06F-012/14 ; G06F-012/16 ; G06F-013/28 ; G06F-015/16 ; G06F-015/173**
File Segment: EPI

7/5/12 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014384763
WPI Acc No: 2002-205466/200226
Related WPI Acc No: 2000-490537; 2001-315873; 2001-367159; 2001-464660; 2001-529143; 2001-569945; 2001-626183; 2002-026065; 2002-062571; 2002-573435
XRPX Acc No: N02-156442

An Internet portal for gathering raw data and presenting meta summarized information to a user has a report processor processing raw data by matching a user request to stored report algorithms

Patent Assignee: YODLEE.COM INC (YODL-N); RAJAN S P (RAJA-I); RANGAN P V (RANG-I); SHARMA M (SHAR-I); WU J (WUJJ-I)
Inventor: RAJAN S P; RANGAN P V; **SHARMA M ; WU J**
Number of Countries: 092 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200131463	A1	20010503	WO 2000US25672	A	20000919	200226 B
AU 200077048	A	20010508	AU 200077048	A	20000919	200226
US 20020078079	A1	20020620	US 99323598	A	19990601	200244
			US 99425626	A	19991022	
EP 1226510	A1	20020731	EP 2000966754	A	20000919	200257

WO 2000US25672 A 20000919
JP 2003514271 W 20030415 WO 2000US25672 A 20000919 200328
JP 2001533529 A 20000919

Priority Applications (No Type Date): US 99425626 A 19991022; US 99323598 A 19990601
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200131463 A1 E 56 G06F-015/00
Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TZ UG ZW
AU 200077048 A Based on patent WO 200131463
US 20020078079 A1 G06F-015/00 CIP of application US 99323598
EP 1226510 A1 E G06F-015/00 Based on patent WO 200131463
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2003514271 W 67 G06F-017/60 Based on patent WO 200131463

Abstract (Basic): WO 200131463 A
NOVELTY - Raw data is gathered from a multiple Internet sites in accordance with the requirements of the selected report algorithm. The raw data is processed into meta summarized information defined by the selected report algorithm. The meta summarized information is then transmitted as a report to a destination associated with the report request. A repository stores aggregated data retrieved for specific users and a check is made of the aggregated data before further data is requested from Internet sites.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of gathering raw data from Internet sites and presenting a requesting user with meta summarized information.
USE - Gathering summary information from user-subscribed web services.
ADVANTAGE - Aggregates data from numerous sources and automatically summarizes that data.
pp; 56 DwgNo 0/10
Title Terms: PORTAL; GATHER; RAW; DATA; PRESENT; META; INFORMATION; USER; REPORT; PROCESSOR; PROCESS; RAW; DATA; MATCH; USER; REQUEST; STORAGE; REPORT; ALGORITHM
Derwent Class: T01
International Patent Class (Main): **G06F-015/00 ; G06F-017/60**
International Patent Class (Additional): **G06F-013/00 ; G06F-017/30**
File Segment: EPI

7/5/13 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014261768 **Image available**
WPI Acc No: 2002-082466/200211
Related WPI Acc No: 2002-255359; 2003-128185
XRPX Acc No: N02-061477
Flow control system for Duplicate Tag store of multiprocessor computer system, suspends issuance of packets to interleaved component, when counter value reaches specified threshold
Patent Assignee: NAGPAL H K (NAGP-I); STEELY S C (STEE-I); VAN DOREN S R (VDOR-I)
Inventor: NAGPAL H K; **STEELY S C ; VAN DOREN S R**
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 20010049742 A1 20011206 US 2000208208 P 20000531 200211 B
US 2000208231 P 20000531

US 2000208439	P	20000531	
US 2000208440	P	20000531	
US 2001867111	A	20010529	

Priority Applications (No Type Date): US 2001867111 A 20010529; US 2000208208 P 20000531; US 2000208231 P 20000531; US 2000208439 P 20000531 ; US 2000208440 P 20000531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010049742	A1		18	G06F-015/16	Provisional application US 2000208208
					Provisional application US 2000208231
					Provisional application US 2000208439
					Provisional application US 2000208440

Abstract (Basic): US 20010049742 A1

NOVELTY - A counter increments, based on issuance of a packet of a class to an interleaved component. A flow control logic (600) suspends the issuance of the packets to the interleaved component, when the counter value reaches a specified threshold.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Flow control method;

(b) Multiprocessor computer system

USE - For preventing overflow of a write storage structure such as first-in-first-out (FIFO) queue in centralized Duplicate Tag store of cache coherent multiprocessor computer system.

ADVANTAGE - The system is protected against failure in pathological traffic patterns, using flow control technique.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic block diagram of quad building block node of a modular, symmetric multiprocessor system.

pp; 18 DwgNo 3/7

Title Terms: FLOW; CONTROL; SYSTEM; DUPLICATE; TAG; STORAGE; MULTIPROCESSOR ; COMPUTER; SYSTEM; SUSPENSION; PACKET; INTERLEAVED; COMPONENT; COUNTER; VALUE; REACH; SPECIFIED; THRESHOLD
Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

7/5/14 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013465370 **Image available**
WPI Acc No: 2000-637313/200061
XRPX Acc No: N00-472611

Hierarchical switch based symmetric multiprocessor system for computer, enables or disables packet transmission from multiprocessor nodes, based on availability of generic and dedicated entry slots of channels

Patent Assignee: COMPAQ COMPUTER CORP (COPQ)
Inventor: **SHARMA M**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6094686	A	20000725	US 97957059	A	19971024	200061	B
			US 98220161	A	19981223		

Priority Applications (No Type Date): US 97957059 A 19971024; US 98220161 A 19981223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6094686	A		73	G06F-015/173	Div ex application US 97957059

Abstract (Basic): US 6094686 A

NOVELTY - A hierarchical switch (155) is coupled to processor nodes

(100a-100h) via data links (170a-170h). A buffer having generic and dedicated entry slots is provided in switch for storing the packets transmitted between nodes via hierarchical channels. A control logic in the switch enables packet transmission from nodes, based on availability of at least one generic and dedicated entry slots of that channel.

DETAILED DESCRIPTION - A destination count register in the switch stores the number of packets associated with specific channel, that are stored in the buffer. A flag register indicates whether the count register value is zero. A transit counter coupled to the buffer, stores count of number of packets that are in transit from source node global port to the buffer. INDEPENDENT CLAIMS are also included for the following:

(a) interface for transferring data in computer system without dead lock;

(b) source nodes and buffer interfacing method

USE - For computer system for high performance application processing.

ADVANTAGE - By coupling SMP nodes to hierarchical switch to form larger SMP system, scalable high performance system can be realized. As the packets are transmitted in certain queues, acknowledgment for packet reception is eliminated, hence bandwidth of the system is enhanced. By monitoring the number of generic and dedicated slots availability, straightforward flow control is implemented to preclude nodes from writing to buffer, after buffer is filled. By tracking number of packets in transit and number of prior cycles in which flow control signal is asserted, use of data link is maximized.

DESCRIPTION OF DRAWING(S) - The figure shows the SMP system.

Processor nodes (100a-100h)

Hierarchical switch (155)

Data links (170a-170h)

pp; 73 DwgNo 7A/36

Title Terms: HIERARCHY; SWITCH; BASED; SYMMETRICAL; MULTIPROCESSOR; SYSTEM; COMPUTER; ENABLE; DISABLE; PACKET; TRANSMISSION; MULTIPROCESSOR; NODE; BASED; AVAILABLE; DEDICATE; ENTER; SLOT; CHANNEL

Derwent Class: T01

International Patent Class (Main): **G06F-015/173**

File Segment: EPI

7/5/15 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

012440507 **Image available**

WPI Acc No: 1999-246615/199921

XRPX Acc No: N99-183723

Architecture and coherency protocol for large symmetric multiprocessing system

Patent Assignee: DIGITAL EQUIP CORP (DIGI); COMPAQ COMPUTER CORP (COPQ)

Inventor: **SHARMA M ; STEELY S C ; VANDOREN S R**

Number of Countries: 027 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 911736	A1	19990428	EP 98308284	A	19981012	199921	B
JP 11282821	A	19991015	JP 98340925	A	19981026	200001	
US 6154816	A	20001128	US 97957565	A	19971024	200063	

Priority Applications (No Type Date): US 97957565 A 19971024

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 911736	A1	E	83	G06F-012/08	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 11282821	A		201	G06F-015/177	
US 6154816	A			G06F-012/16	

Abstract (Basic): EP 911736 A1

NOVELTY - A hierarchical switch structure allows for a number of multiprocessor nodes (12a,12b,12c,12d) to be coupled to the switch. Each multiprocessor node (12a,12b,12c,12d) includes a simultaneous buffering system which allows all processors of the multiprocessor node to operate at peak performance.

DETAILED DESCRIPTION - A hierarchical switch structure allows for a number of multiprocessor nodes (12a,12b,12c,12d) to be coupled to the switch. Within each multiprocessor node, a simultaneous buffering system allows all the processors of the multiprocessor node to operate at peak performance. A memory (13) is shared amongst the nodes, with a portion of the memory (13a,13b,13c,13d) resident at each of the multiprocessor nodes. Each of the multiprocessor nodes includes a number of elements for maintaining memory coherency, including a victim cache, a directory and a transaction tracking table. INDEPENDENT CLAIMS are included for; a multi-processing system comprising of multiple nodes coupled via a switch; a method for allowing multiple references to a common block in a shared memory to be executing simultaneously in a multiprocessing system.

USE - Low occupancy protocol for managing concurrent transactions with dependencies.

ADVANTAGE - In which victim cache allows for selective updates of victim data destined for memory stored at remote multiprocessing nodes, thereby improving overall memory performance.

DESCRIPTION OF DRAWING(S) - The drawing shows an embodiment of a multiprocessor computer node of the invention comprising a switch.

Multiprocessor nodes (10)
Processor modules (12a,12b,12c,12d)
Memory modules (13a,13b,13c,13d)
I/O processor module (14)
I/O bus (14a)
Quad Switch Address control chip (18)
Quad switch data slice chip (19)
Duplicate tag store (20)
pp; 83 DwgNo 2/36

Title Terms: ARCHITECTURE; COHERE; PROTOCOL; SYMMETRICAL; MULTIPROCESSOR; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-012/08 ; G06F-012/16 ; G06F-015/177**
International Patent Class (Additional): **G06F-015/16 ; G06F-015/167**
File Segment: EPI

7/5/16 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012440504 **Image available**
WPI Acc No: 1999-246612/199921
XRPX Acc No: N99-183720

Architecture and coherency protocol for large symmetric multiprocessing system

Patent Assignee: DIGITAL EQUIP CORP (DIGI); COMPAQ COMPUTER CORP (COPQ)
Inventor: FENWICK D M; **SHARMA M ; STEELY S C ; VANDOREN S R**
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 911731	A2	19990428	EP 98308323	A	19981012	199921	B
JP 11282820	A	19991015	JP 98340924	A	19981026	200001	
US 6122714	A	20000919	US 97957298	A	19971024	200048	

Priority Applications (No Type Date): US 97957298 A 19971024
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 911731	A2	E	75	G06F-009/46	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT

LI LT LU LV MC MK NL PT RO SE SI
JP 11282820 A 199 G06F-015/177
US 6122714 A G06F-012/16

Abstract (Basic): EP 911731 A2

NOVELTY - A transaction tracking table (TTT) is maintained at each of the multiprocessor nodes, and is used to determine the order of requests that are returned to the multiprocessing node.

DETAILED DESCRIPTION - A hierarchical switch structure allows for a number of multiprocessor nodes (12a,12b,12c,12d) to be coupled to the switch. Within each multiprocessor node, a simultaneous buffering system allows all the processors of the multiprocessor node to operate at peak performance. A memory (13) is shared amongst the nodes, with a portion of the memory (13a,13b,13c,13d) resident at each of the multiprocessor nodes. A tracking mechanism is associated with each of the multiprocessing nodes (12a,12b,12c,12d), for identifying a position of a request to an address of a remote portion of shared memory (13a,13b,13c,13d) issued by one of the processors in the multiprocessor nodes, relative to a number of other requests issued to the address by the processor in the coupled processor nodes. INDEPENDENT CLAIMS are included for; a method for maintaining order between a number of requests issued to a common address in a multiprocessor system.

USE - Order support mechanism for use in switch based multiprocessor system.

ADVANTAGE - Transaction tracking table ensures that latency of operations is minimized. Provides large communications bandwidth, low controller occupancy, and can scale to large number of processor.

DESCRIPTION OF DRAWING(S) - The drawing shows an embodiment of a multiprocessor computer node of the invention comprising a switch.

Multiprocessor nodes (10)
Processor modules (12a,12b,12c,12d)
Memory modules (13a,13b,13c,13d)
I/O processor module (14)
I/O bus (14a)
Quad Switch Address control chip (18)
Quad switch data slice chip (19)
Duplicate tag store (20)
pp; 75 DwgNo 2/36

Title Terms: ARCHITECTURE; COHERE; PROTOCOL; SYMMETRICAL; MULTIPROCESSOR; SYSTEM
Derwent Class: T01
International Patent Class (Main): **G06F-009/46 ; G06F-012/16 ; G06F-015/177**
International Patent Class (Additional): **G06F-012/08 ; G06F-015/16 ; G06F-015/167**
File Segment: EPI

7/5/17 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012103695 **Image available**
WPI Acc No: 1998-520607/199844
XRPX Acc No: N98-406620

Object oriented network protocol events managing system for computer network - has network protocol event object which is derived from protocol event class and specifies protocol event types from two sets of event types in object

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: **SHARMA M** ; TURNER L B; YEUNG L Y T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5809235	A	19980915	US 96612740	A	19960308	199844	B

Priority Applications (No Type Date): US 96612740 A 19960308

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 5809235 A 38 G06F-015/16

Abstract (Basic): US 5809235 A

The system includes a network protocol event class object which includes a first set of network protocol event types, i.e. class definitions, which occur at multiple protocol layers. The class object also includes a second set of network protocol event types which occur at specific protocol layers.

A network protocol event object is derived from the network protocol event class which specifies network protocol event types from the two sets of monitoring by an application in the network. Events of the specified network protocol event types are stored in the event objects as the event occurs in the network. Upon request, the stored events are sent to the application.

USE: - For LAN, WAN

ADVANTAGE - Manages execution threads, dynamically to maximise performance. Provides efficient control over reuse of programs.

Dwg.1/10

Title Terms: OBJECT; ORIENT; NETWORK; PROTOCOL; EVENT; MANAGE; SYSTEM; COMPUTER; NETWORK; NETWORK; PROTOCOL; EVENT; OBJECT; DERIVATIVE; PROTOCOL ; EVENT; CLASS; SPECIFIED; PROTOCOL; EVENT; TYPE; TWO; SET; EVENT; TYPE; OBJECT
Derwent Class: T01
International Patent Class (Main): **G06F-015/16**
File Segment: EPI

7/5/18 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011930982 **Image available**
WPI Acc No: 1998-347892/199830
XRPX Acc No: N98-271582

Object oriented communication interface unit in computer network - establishes communication path in protocol stack, between remote communication endpoints through selected newly created protocol interface object and protocol layer objects

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HEIMSOTH D D; HORN G R; **SHARMA M** ; TURNER L B; YEUNG L Y T
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 5764915 A 19980609 US 96611849 A 19960308 199830 B

Priority Applications (No Type Date): US 96611849 A 19960308
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 5764915 A 38 G06F-013/14

Abstract (Basic): US 5764915 A

The interface unit creates a new instant of network address object from a network address class object to define a local communication endpoint in response to communication request signal. A new set of protocol layer is created from respective protocol layer class object and binding the new protocol layer to form an object based protocol stack for local communication endpoint. New set of protocol interface objects are created each from respective protocol interface class object.

Each newly created protocol interface object with a corresponding newly created protocol layer object, provides external interface for requesting application to each of the newly created protocol layer object. The newly created protocol interface object are called selectively from the local communication endpoint to establish the communication path between remote communication endpoints through the

selected newly created protocol interface object and protocol layer object, in the protocol stack.

ADVANTAGE - Develops several protocol layer from same set of protocol class objects, efficiently. Establishes communication path in protocol stack reliably.

Dwg.4B/10

Title Terms: OBJECT; ORIENT; COMMUNICATE; INTERFACE; UNIT; COMPUTER; NETWORK; ESTABLISH; COMMUNICATE; PATH; PROTOCOL; STACK; REMOTE; COMMUNICATE; THROUGH; SELECT; NEW; PROTOCOL; INTERFACE; OBJECT; PROTOCOL; LAYER; OBJECT

Derwent Class: T01

International Patent Class (Main): **G06F-013/14**

International Patent Class (Additional): **G06F-015/173**

File Segment: EPI

7/5/19 (Item 16 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011895931 **Image available**

WPI Acc No: 1998-312841/199827

XRPX Acc No: N98-245190

Voice recognition system for e.g. transaction operations - has client terminal with voice input obtaining speech data and processor which provides information concerning voice recognition between input speech data and user information from data base

Patent Assignee: T-NETIX INC (TNET-N); DEVINNEY E J (DEVI-I); KEYSER C (KEYS-I); MAMMONE R J (MAMM-I); ROTHACKER R (ROTH-I); SHARMA M (SHAR-I)

Inventor: DEVINNEY E J; KEYSER C; MAMMONE R J; ROTHACKER R; **SHARMA M**

Number of Countries: 079 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9823062	A1	19980528	WO 97US21259	A	19971121	199827	B
AU 9873047	A	19980610	AU 9873047	A	19971121	199843	
EP 938793	A1	19990901	EP 97949507	A	19971121	199940	
			WO 97US21259	A	19971121		
CN 1244984	A	20000216	CN 97181428	A	19971121	200027	
JP 2001505688	W	20010424	WO 97US21259	A	19971121	200130	
			JP 98523888	A	19971121		
US 20030046083	A1	20030306	US 9631638	P	19961122	200320	
			US 97976279	A	19971121		

Priority Applications (No Type Date): US 9631638 P 19961122; US 97976279 A 19971121

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9823062	A1	E	51	H04L-012/22	
Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW				
Designated States (Regional): AT BE CH DE DK EA ES FI FR GB GH GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 9873047	A				Based on patent WO 9823062
EP 938793	A1	E			Based on patent WO 9823062
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
CN 1244984	A			H04L-012/22	
JP 2001505688	W		55	G06F-015/00	Based on patent WO 9823062
US 20030046083	A1			G10L-021/00	Provisional application US 9631638

Abstract (Basic): WO 9823062 A

The system includes a client terminal with a voice input obtaining speech data and two communications units. The first unit is connected to the voice input and transmitting information concerning the speech data.

A voice recognition system receives information from a voice information database and comprises a second communication unit receiving the information concerning the speech data from the first communication unit. A processing unit provides information concerning voice recognition between the input speech data and the user information from the voice information database.

USE - E.g. for computer-related credit card transaction security for use e.g. with Internet, for prison inmate transactions, database access requests, internet transactions.

ADVANTAGE - Increases security by using personal characteristics of user for identifying and verifying user.

Dwg.7/12

Title Terms: VOICE; RECOGNISE; SYSTEM; TRANSACTION; OPERATE; CLIENT; TERMINAL; VOICE; INPUT; OBTAIN; SPEECH; DATA; PROCESSOR; INFORMATION; VOICE; RECOGNISE; INPUT; SPEECH; DATA; USER; INFORMATION; DATA; BASE

Derwent Class: P86; T01; T05; W04

International Patent Class (Main): **G06F-015/00** ; G10L-021/00; H04L-012/22

International Patent Class (Additional): **G06F-017/60** ; **G06F-019/00** ; G10L-005/00; G10L-015/00; G10L-017/00

File Segment: EPI; EngPI

7/5/20 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011459750 **Image available**

WPI Acc No: 1997-437657/199741

XRPX Acc No: N97-363812

Object oriented dynamic thread management for high performance server - involves having control process that uses variable parameters to limit number of active threads overall and per client

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)

Inventor: **SHARMA M** ; YEUNG L Y T

Number of Countries: 006 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 794490	A2	19970910	EP 97300612	A	19970130	199741	B
JP 9265409	A	19971007	JP 9740713	A	19970225	199750	
KR 97068308	A	19971013	KR 9662995	A	19961209	199843	
US 6182109	B1	20010130	US 96613106	A	19960308	200108	
KR 253930	B1	20000415	KR 9662995	A	19961209	200124	
JP 3229237	B2	20011119	JP 9740713	A	19970225	200176	

Priority Applications (No Type Date): US 96613106 A 19960308

Cited Patents: No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 794490	A2	E	48	G06F-009/46	
Designated States (Regional): DE FR GB					
JP 9265409	A		38	G06F-009/46	
KR 97068308	A			H04L-012/28	
US 6182109	B1			G06F-009/00	
KR 253930	B1			G06F-009/46	
JP 3229237	B2		38	G06F-009/46	Previous Publ. patent JP 9265409

Abstract (Basic): EP 794490 A

The dynamic thread management method involves allocating minimum and maximum execution units in communication process pool necessary to support client load. When a client needs to make requests of the server a connection is established and can involve creating threads to manage the connection. At any time the servers operating system multi-tasks the threads to maintain and service the client requests.

A management process has a number of parameters. These define the minimum number of threads at server start-up, maximum number to be allocated both overall and to any one client. As a client request needs a new thread these parameters control the use of resources.

ADVANTAGE - Manages system resources to provide admission control for normal and session client requests.

Dwg.1/10

Title Terms: OBJECT; ORIENT; DYNAMIC; THREAD; MANAGEMENT; HIGH; PERFORMANCE ; SERVE; CONTROL; PROCESS; VARIABLE; PARAMETER; LIMIT; NUMBER; ACTIVE; THREAD; OVERALL; PER; CLIENT

Derwent Class: T01; W01

International Patent Class (Main): **G06F-009/00** ; **G06F-009/46** ; H04L-012/28

International Patent Class (Additional): **G06F-013/00** ; **G06F-015/16** ; **G06F-015/173** ; H04L-029/06

File Segment: EPI

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Set     Items   Description
S1       6209   AU=(STEELY, S? OR STEELY S? OR SHARMA, M? OR SHARMA M? OR -
            VANDORN, S? OR VANDORN S? OR VAN DORN, S? OR VAN DORN S?)
S2          0   S1 AND (INTERNODE? OR INTER()NODE? OR NODE?)()SWITCH??
S3          0   S1 AND MULTIPLE()PROCESSOR?
File   2:INSPEC 1969-2004/May W5
         (c) 2004 Institution of Electrical Engineers
File   6:NTIS 1964-2004/Jun W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2004/May W5
         (c) 2004 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2004/May W5
         (c) 2004 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jun W1
         (c) 2004 BLDSC all rts. reserv.
File  92:IHS Intl.Stds.& Specs. 1999/Nov
         (c) 1999 Information Handling Services
File  94:JICST-EPlus 1985-2004/May W3
         (c)2004 Japan Science and Tech Corp(JST)
File  95:TEME-Technology & Management 1989-2004/May W4
         (c) 2004 FIZ TECHNIK
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/May
         (c) 2004 The HW Wilson Co.
File 103:Energy SciTec 1974-2004/May B2
         (c) 2004 Contains copyrighted material
File 144:Pascal 1973-2004/May W5
         (c) 2004 INIST/CNRS
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
         (c) 2004 EBSCO Publishing
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
         (c) 2003 EBSCO Pub.
File 239:Mathsci 1940-2004/Jul
         (c) 2004 American Mathematical Society
File 275:Gale Group Computer DB(TM) 1983-2004/Jun 09
         (c) 2004 The Gale Group
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File 647:CMP  Computer Fulltext 1988-2004/May W5
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/May W5
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jun 08
         (c) 2004 The Dialog Corp.
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